[FIG. 1]

Structure of a conventional parallel processor

FIG.1 PRIOR ART
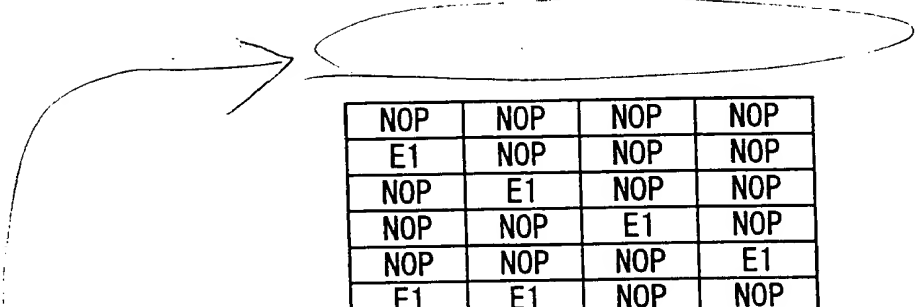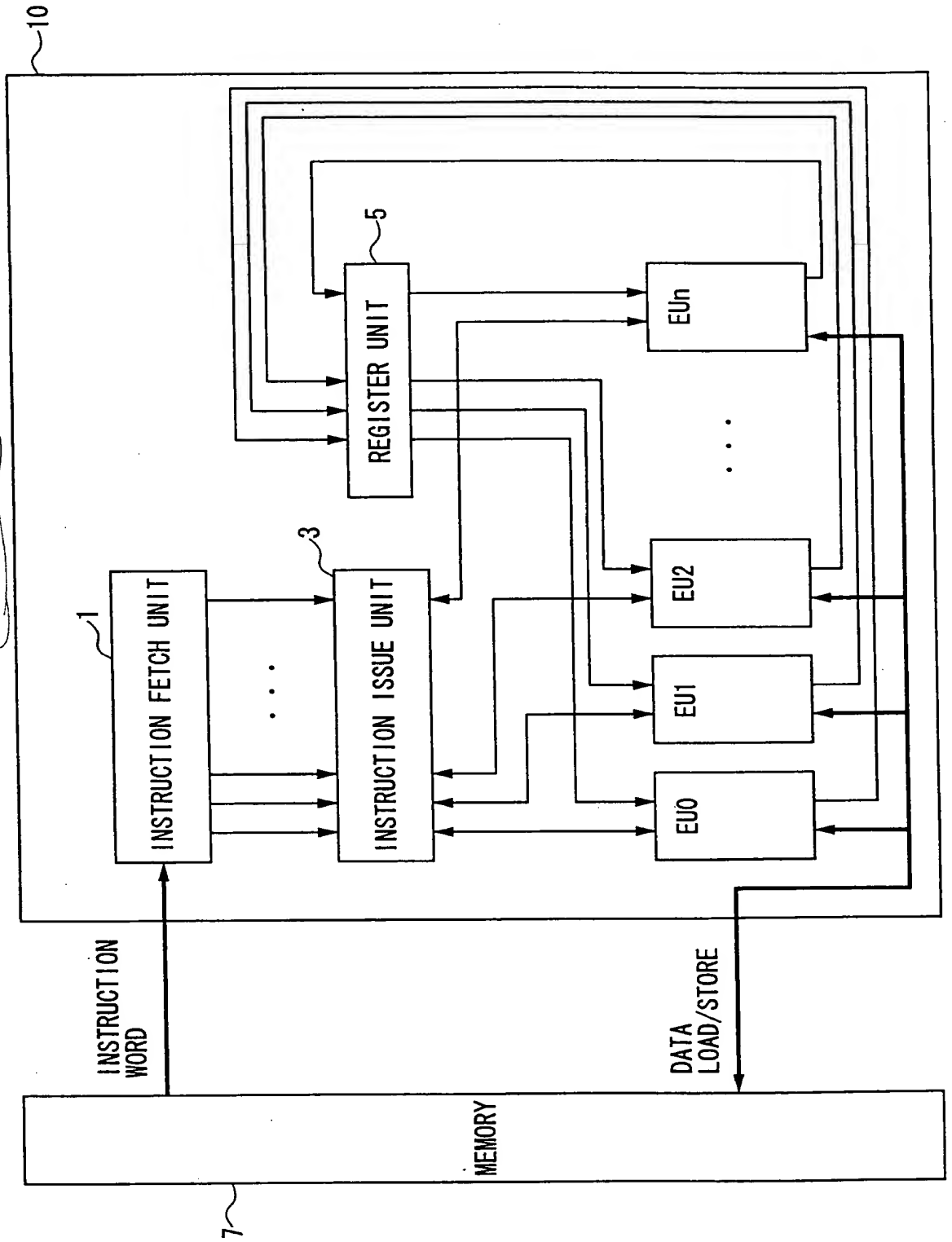
FIG.2

NOP	NOP	NOP	NOP
E1	NOP	NOP	NOP
NOP	E1	NOP	NOP
NOP	NOP	E1	NOP
NOP	NOP	NOP	E1
E1	E1	NOP	NOP
E1	NOP	E1	NOP
E1	NOP	NOP	E1
NOP	E1	E1	NOP
NOP	E1	NOP	E1
NOP	NOP	E1	E1
E1	E1	E1	NOP
E1	E1	NOP	E1
E1	NOP	E1	E1
NOP	E1	E1	E1
E1	E1	E1	E1

[FIG. 2]

Formats of instruction words to be supplied to a conventional parallel processor having four instruction execution units

[FIG. 3]

Structure of a first example of a parallel processor in accordance with a first embodiment of the present invention
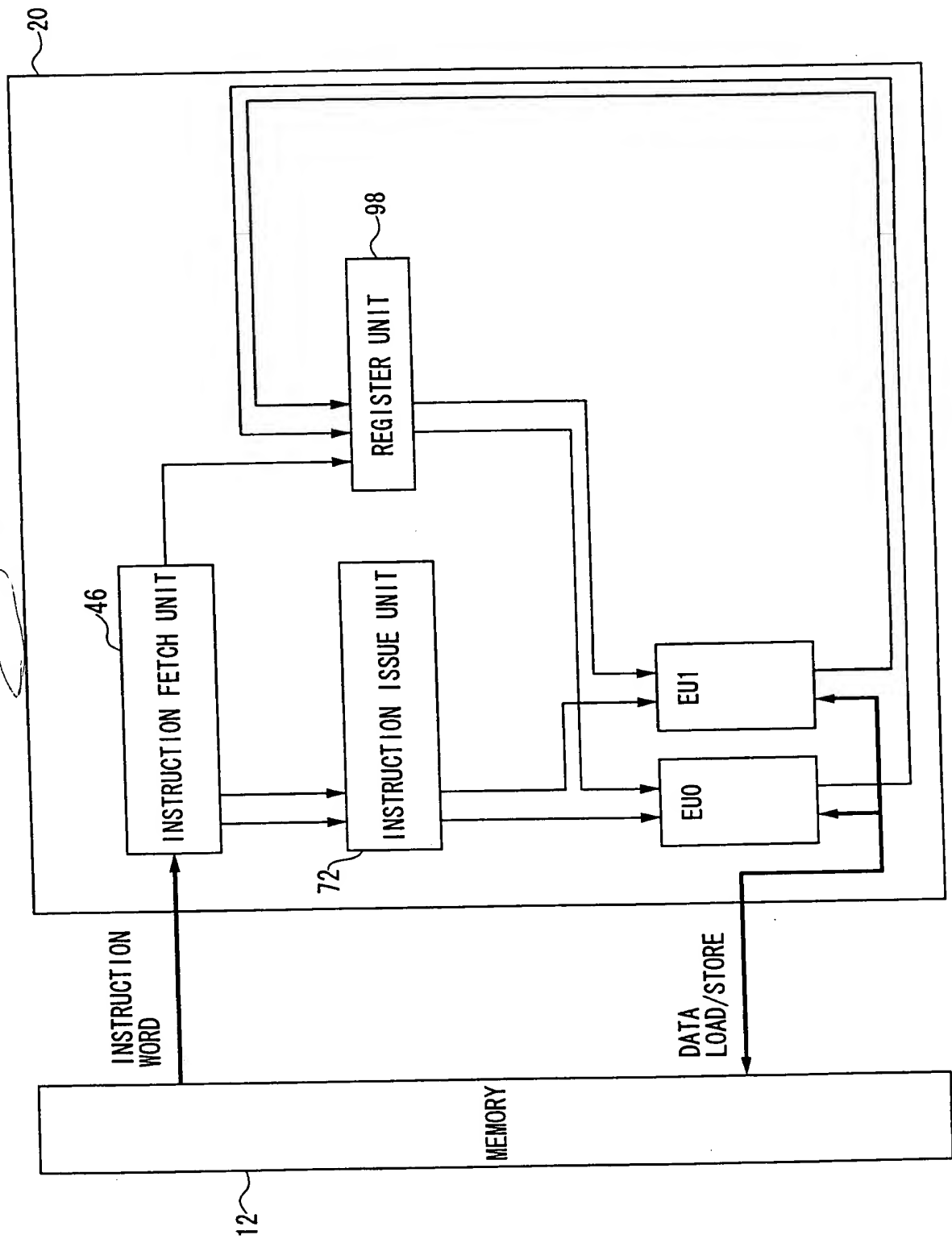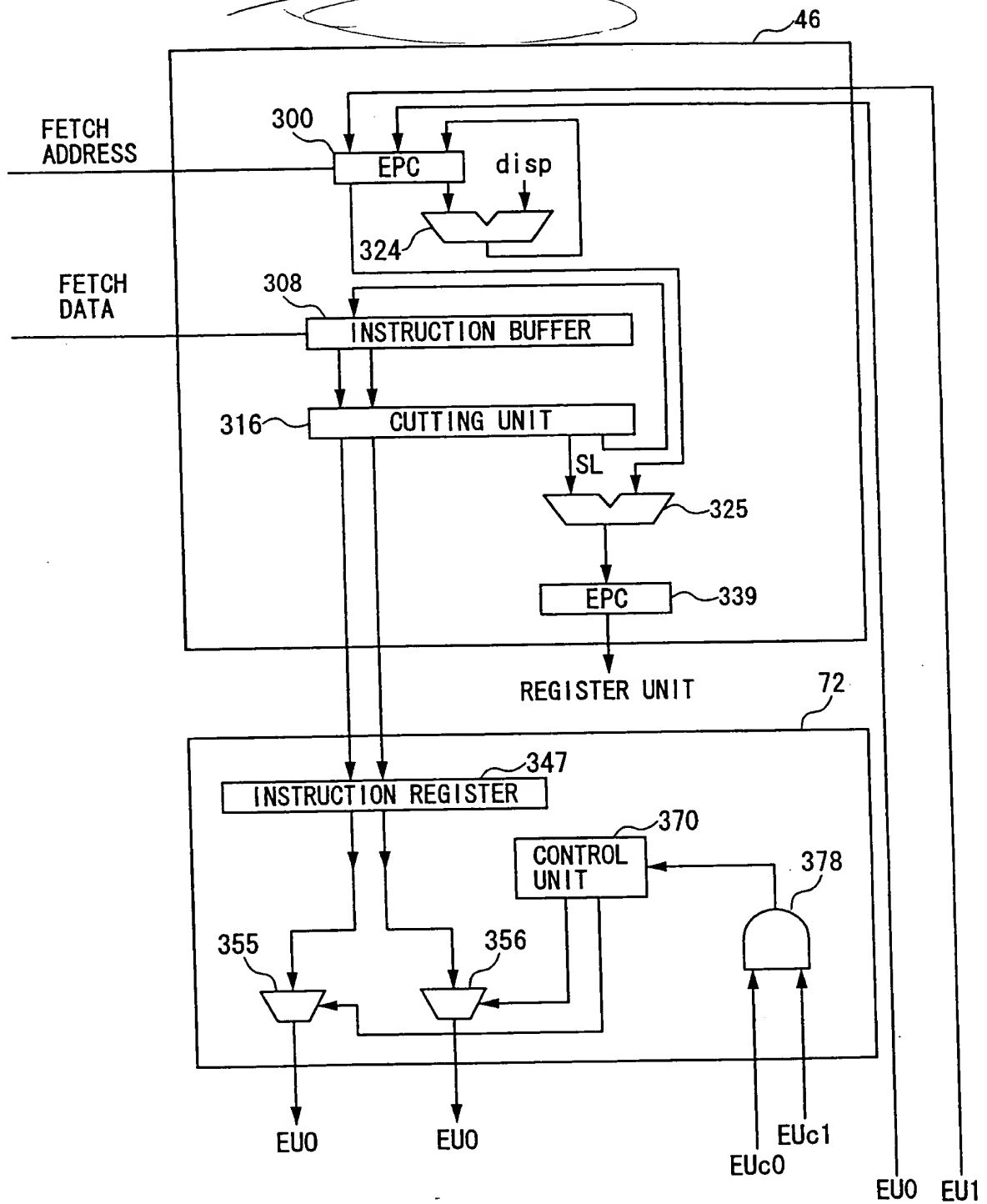
FIG.3

MEMORY

INSTRUCTION WORD

DATA LOAD/STORE

INSTRUCTION FETCH UNIT

INSTRUCTION ISSUE UNIT

REGISTER UNIT

EU1

EU0

20

46

72

98

12

FIG.4

46

FETCH
ADDRESS ──────────────→ 300

EPC   disp

324

FETCH
DATA ──────────────→ 308

INSTRUCTION BUFFER

316 ── CUTTING UNIT

SL

325

EPC ── 339

REGISTER UNIT   72

INSTRUCTION REGISTER ── 347

CONTROL UNIT ── 370

378

355   356

EU0   EU0   EUc0 EUc1   EU0 EU1
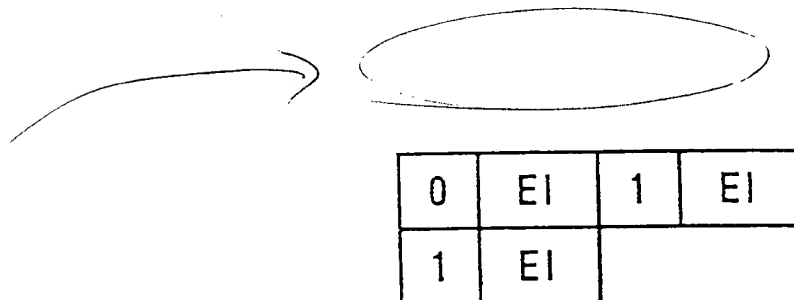
[FIG. 4]

Structures of an instruction fetch unit and an

instruction issue unit of the parallel processor shown

in FIG. 3

FIG. 5

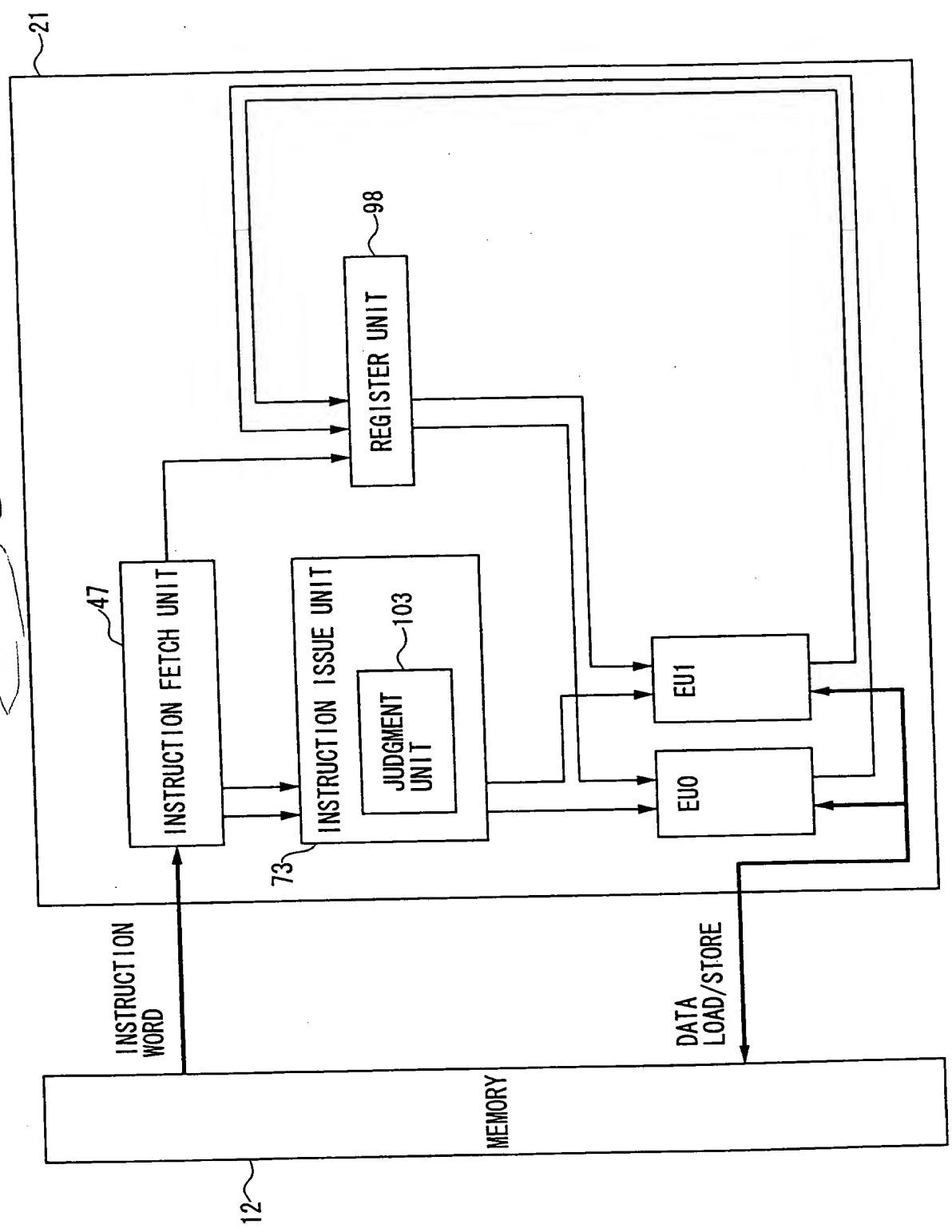| 0	EI	1	EI
1	EI		

[FIG. 5]

Formats of instruction words to be supplied to the
parallel processor of the first embodiment of the
present invention

[FIG. 6]

Structure of a second example of the parallel processor in accordance with the first embodiment of the present invention

FIG.6

21

47 INSTRUCTION FETCH UNIT

73 INSTRUCTION ISSUE UNIT

JUDGMENT UNIT 103

98 REGISTER UNIT

EU1

EU0

INSTRUCTION WORD

DATA LOAD/STORE

MEMORY

12

[FIG. 7]

Structure of a first example of a parallel processor in
accordance with a second embodiment of the present
invention

FIG.7

```
MEMORY ──12
  │
  │ INSTRUCTION
  │ WORD
  ▼
┌─────────────────────────────────────────────────────── 22
│                                                              
│  ┌──────────────────────┐ ──48                              
│  │ INSTRUCTION FETCH UNIT│                    ┌──────────────┐
│  │  ┌────────────────┐   │                    │ REGISTER UNIT│──99
│  │  │  CONVERSION    │   │                    └──────────────┘
│  │  │    UNIT        │───115                                  
│  │  └────────────────┘   │                                   
│  └──────────────────────┘                                    
│         │                                                     
│         ▼                                                     
│  ┌──────────────────────┐ ──74                               
│  │ INSTRUCTION ISSUE UNIT│                                    
│  └──────────────────────┘                                    
│                                                               
│  ┌─────┐ ┌─────┐ ┌─────┐ ┌─────┐ ┌─────┐ ┌─────┐             
│  │ LU0 │ │ IU0 │ │ IU1 │ │ FU0 │ │ FU1 │ │ BU0 │             
│  └─────┘ └─────┘ └─────┘ └─────┘ └─────┘ └─────┘             
│                                                               
└───────────────────────────────────────────────────────
   │
   │ DATA
   │ LOAD/STORE
```

FIG.8

FETCH ADDRESS

301 EPC   disp

326

FETCH DATA

309 INSTRUCTION BUFFER

317 CUTTING UNIT

SL

327

CONVERSION UNIT

115

EPC   340

REGISTER UNIT   74

353 INSTRUCTION REGISTER

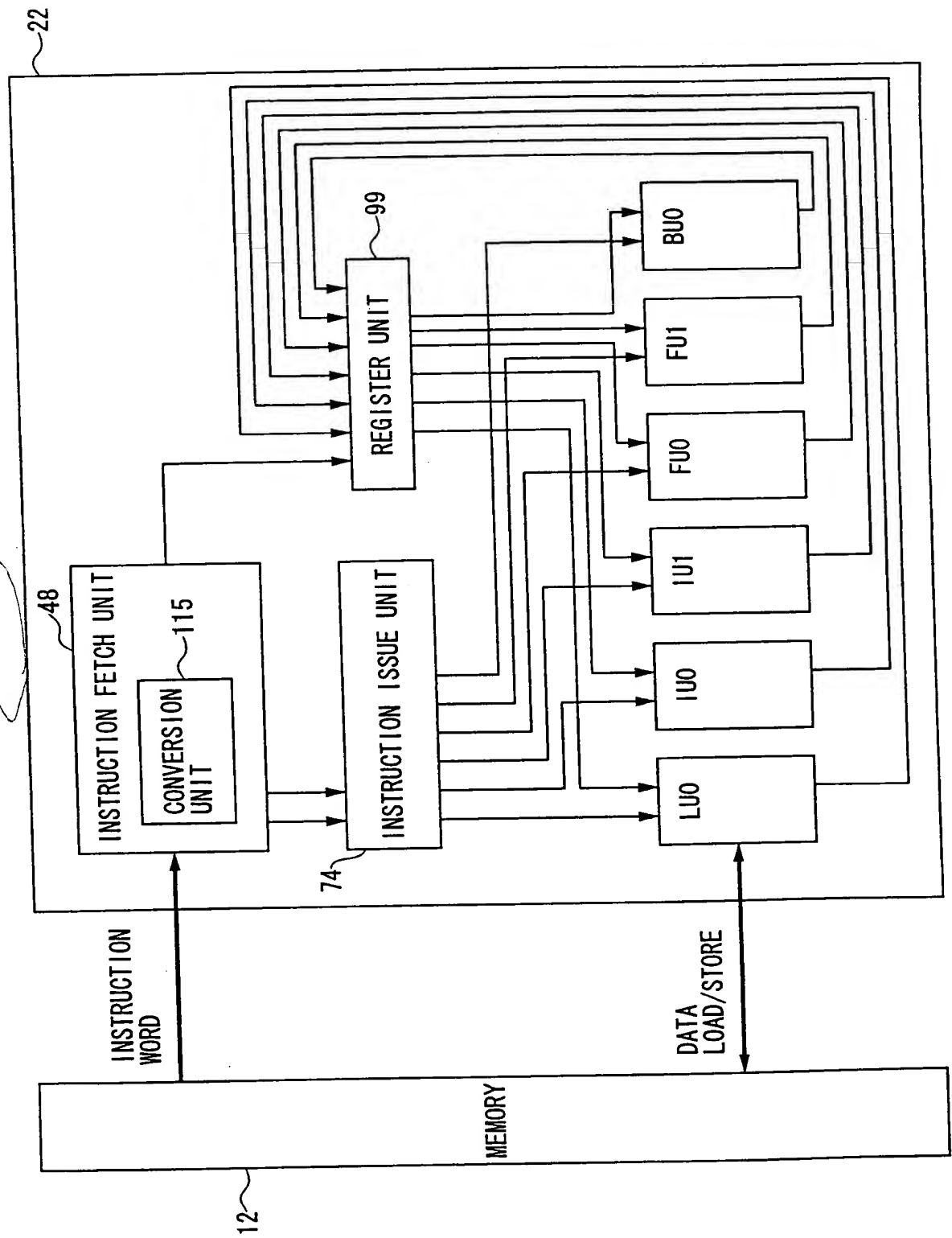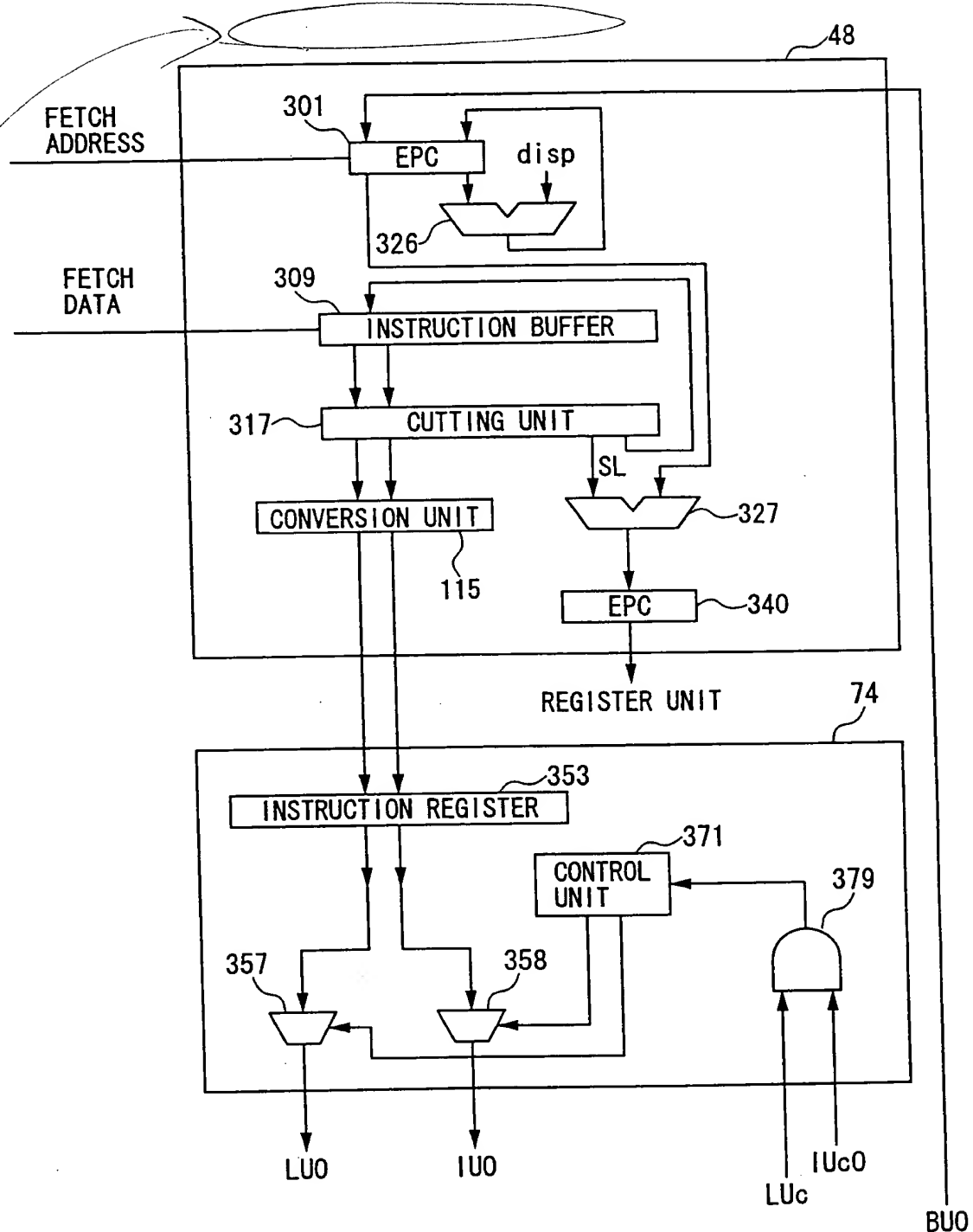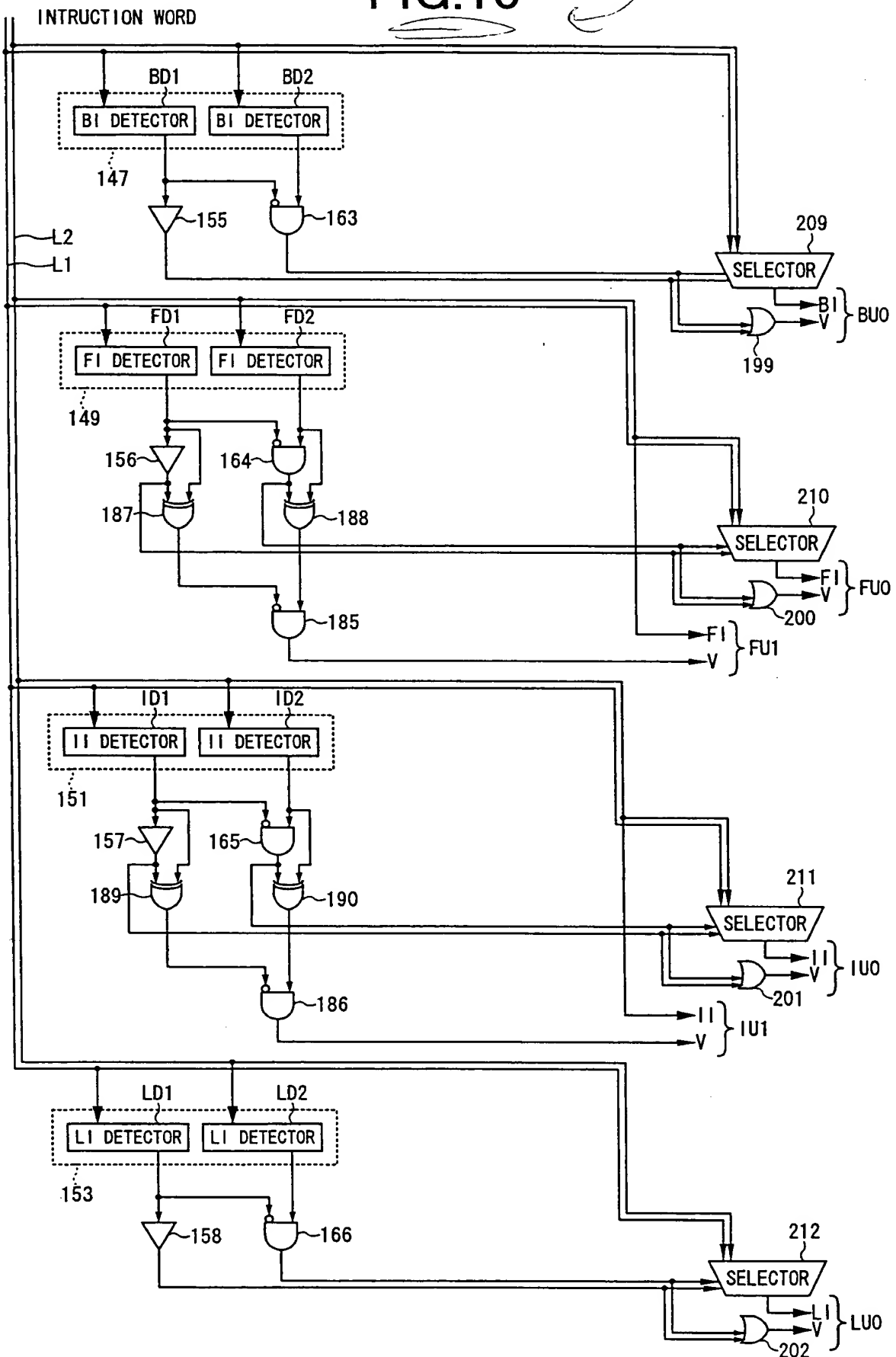371 CONTROL UNIT   379

357   358

LU0   IU0   IUc0

LUc   BU0

[FIG. 8]

Structures of an instruction fetch unit and an instruction issue unit of the parallel processor shown in FIG. 7
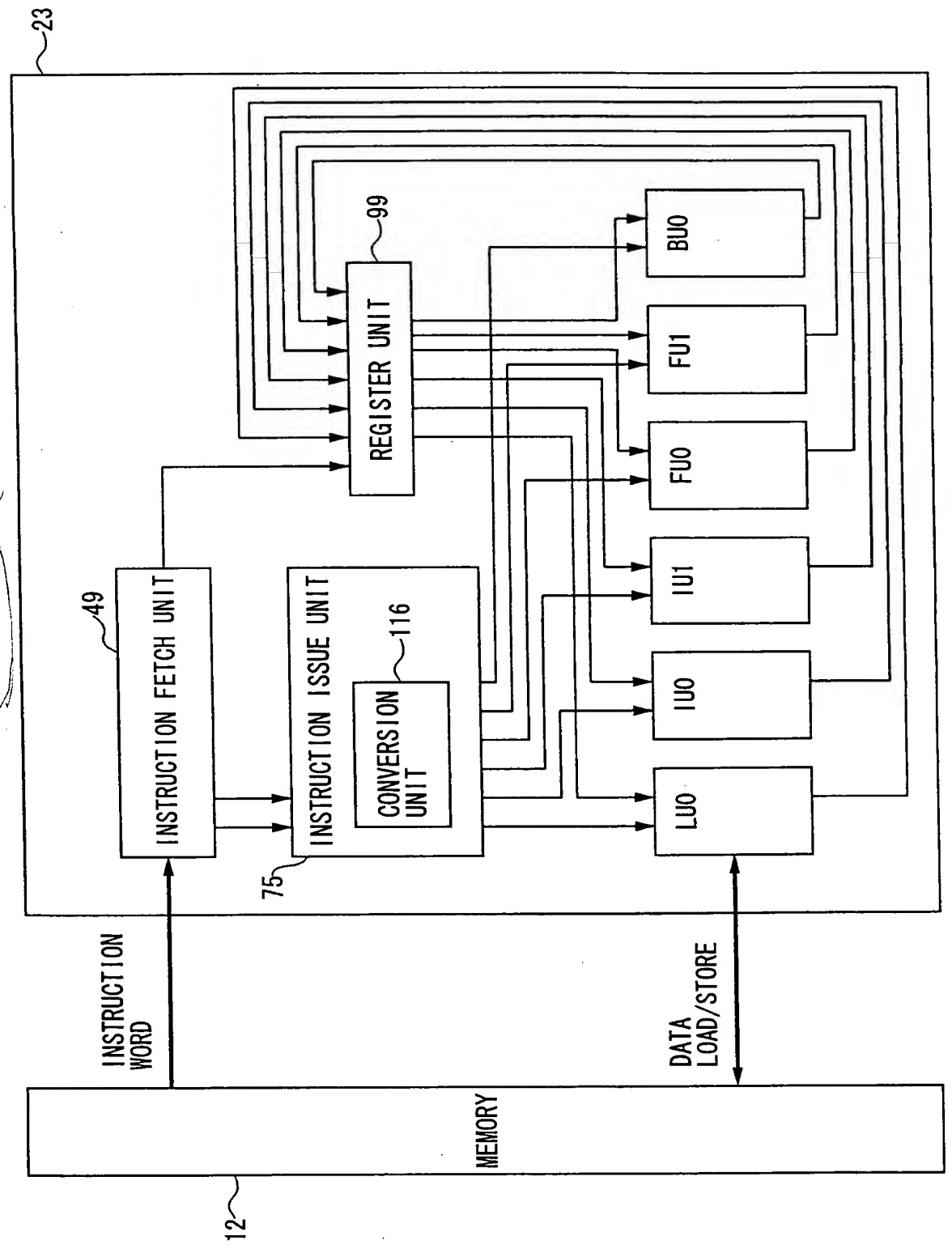
FIG. 9

Basic instruction rearrangement in the parallel processor of the second embodiment of the present invention

FORMAT OF INSTRUCTION WORDS (13)				LU0		IU0		IU1		FU0		FU1		BU0	
				V	LI	V	II	V	II	V	FI	V	FI	V	BI
0	BI	1	FI	0	—	0	—	0	—	1	FI	0	—	1	BI
0	BI	1	II	0	—	1	II	0	—	0	—	0	—	1	BI
0	BI	1	LI	1	LI	0	—	0	—	0	—	0	—	1	BI
0	FI	1	BI	0	—	0	—	0	—	1	FI	0	—	1	BI
0	FI	1	FI	0	—	0	—	0	—	1	FI	1	FI	0	—
0	FI	1	II	0	—	1	II	0	—	1	FI	0	—	0	—
0	FI	1	LI	1	LI	0	—	0	—	1	FI	0	—	0	—
0	II	1	BI	0	—	1	II	0	—	0	—	0	—	1	BI
0	II	1	FI	0	—	1	II	0	—	1	FI	0	—	0	—
0	II	1	II	0	—	1	II	1	II	0	—	0	—	0	—
0	II	1	LI	1	LI	1	II	0	—	0	—	0	—	0	—
0	LI	1	BI	1	LI	0	—	0	—	0	—	0	—	1	BI
0	LI	1	FI	1	LI	0	—	0	—	1	FI	0	—	0	—
0	LI	1	II	1	LI	1	II	0	—	0	—	0	—	0	—
1	BI			0	—	0	—	0	—	0	—	0	—	1	BI
1	FI			0	—	0	—	0	—	1	FI	0	—	0	—
1	II			0	—	1	II	0	—	0	—	0	—	0	—
1	LI			1	LI	0	—	0	—	0	—	0	—	0	—

(15) (17)

[FIG. 10]

Circuit diagram of a conversion unit in the parallel

processor shown in FIG. 7

FIG.10

[FIG. 11]

Circuit diagram of the conversion unit in a case where

the maximum basic instruction word length is 4

FIG.11
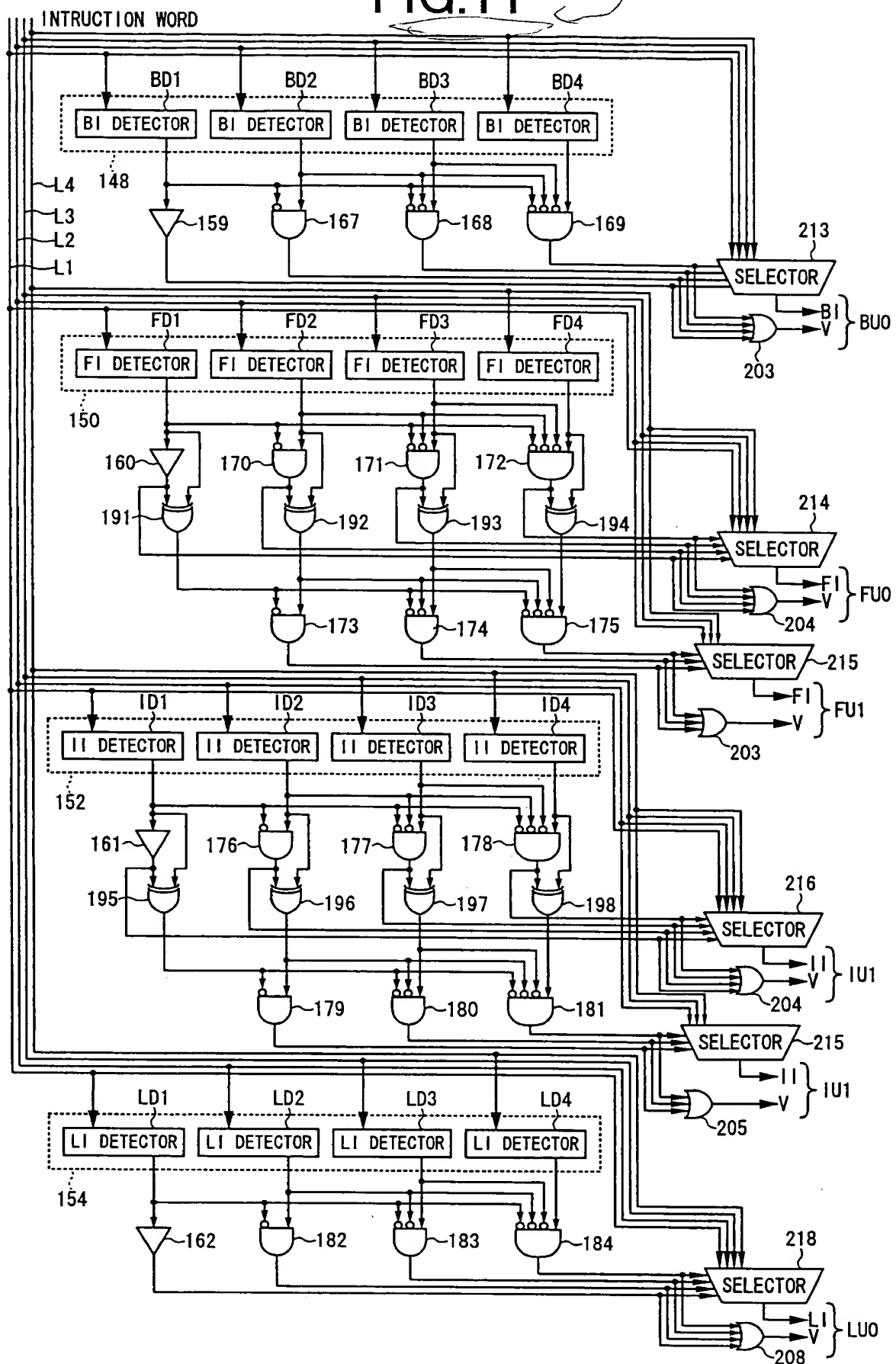
INTRUCTION WORD

[FIG. 12]

Structure of a second example of the parallel processor

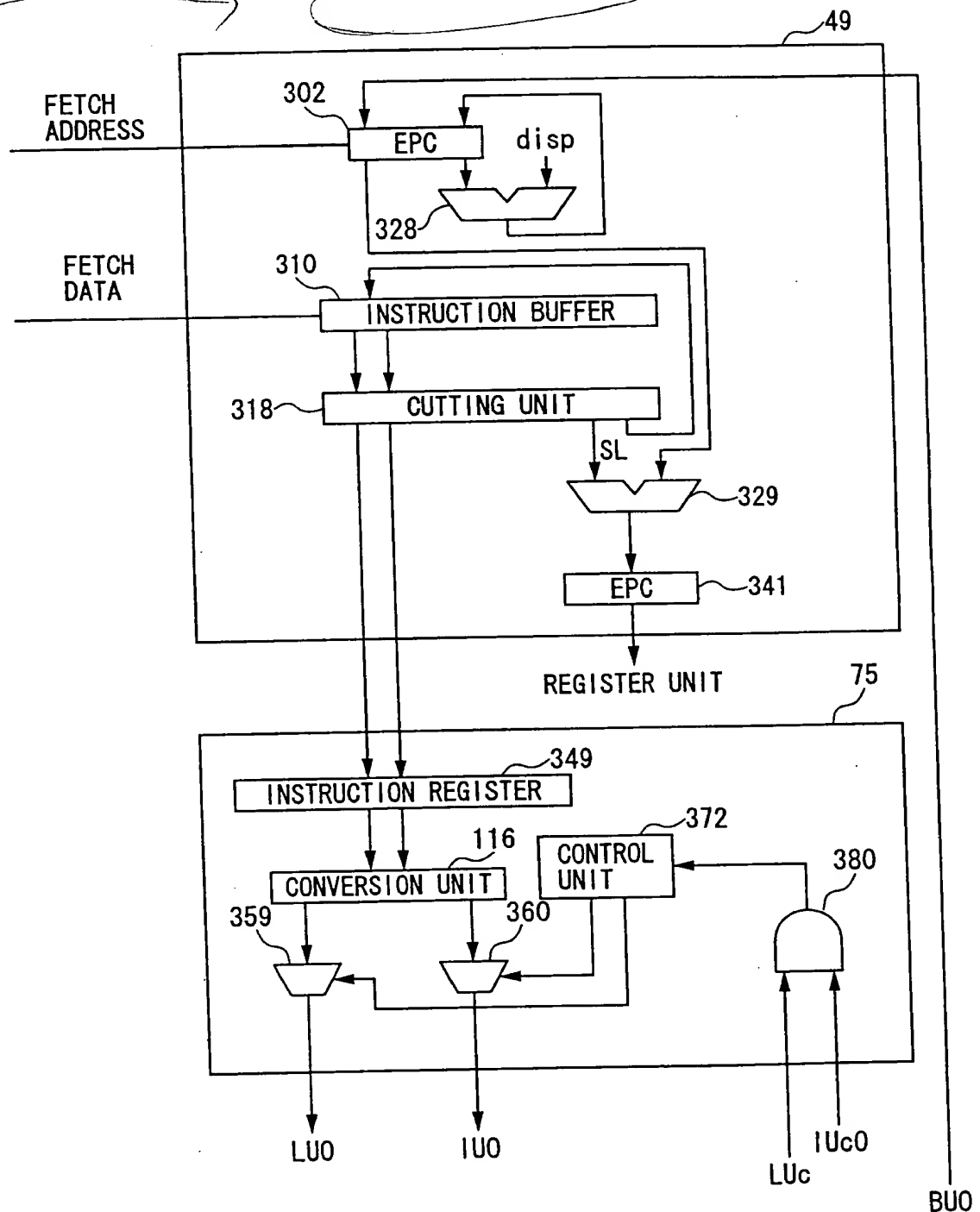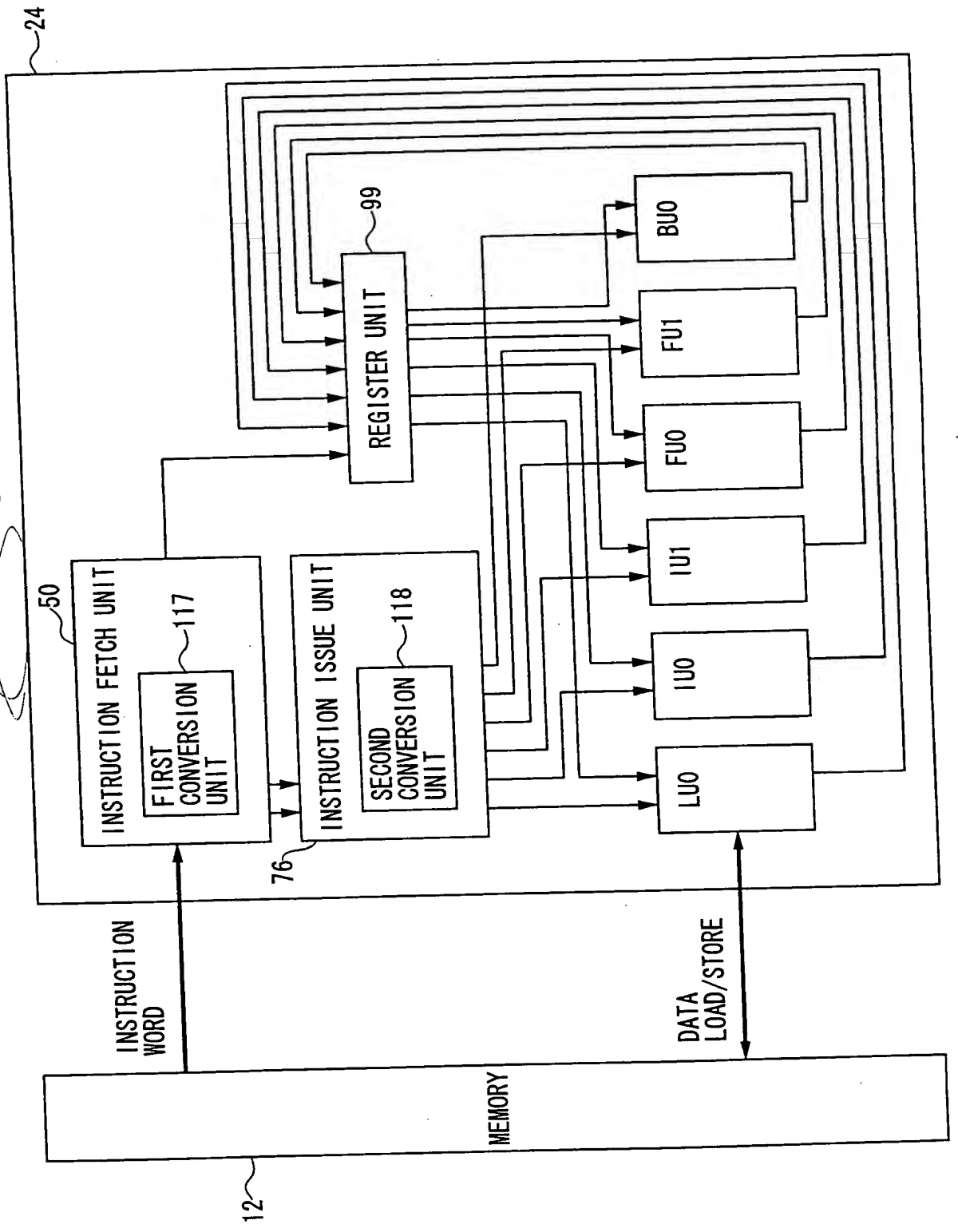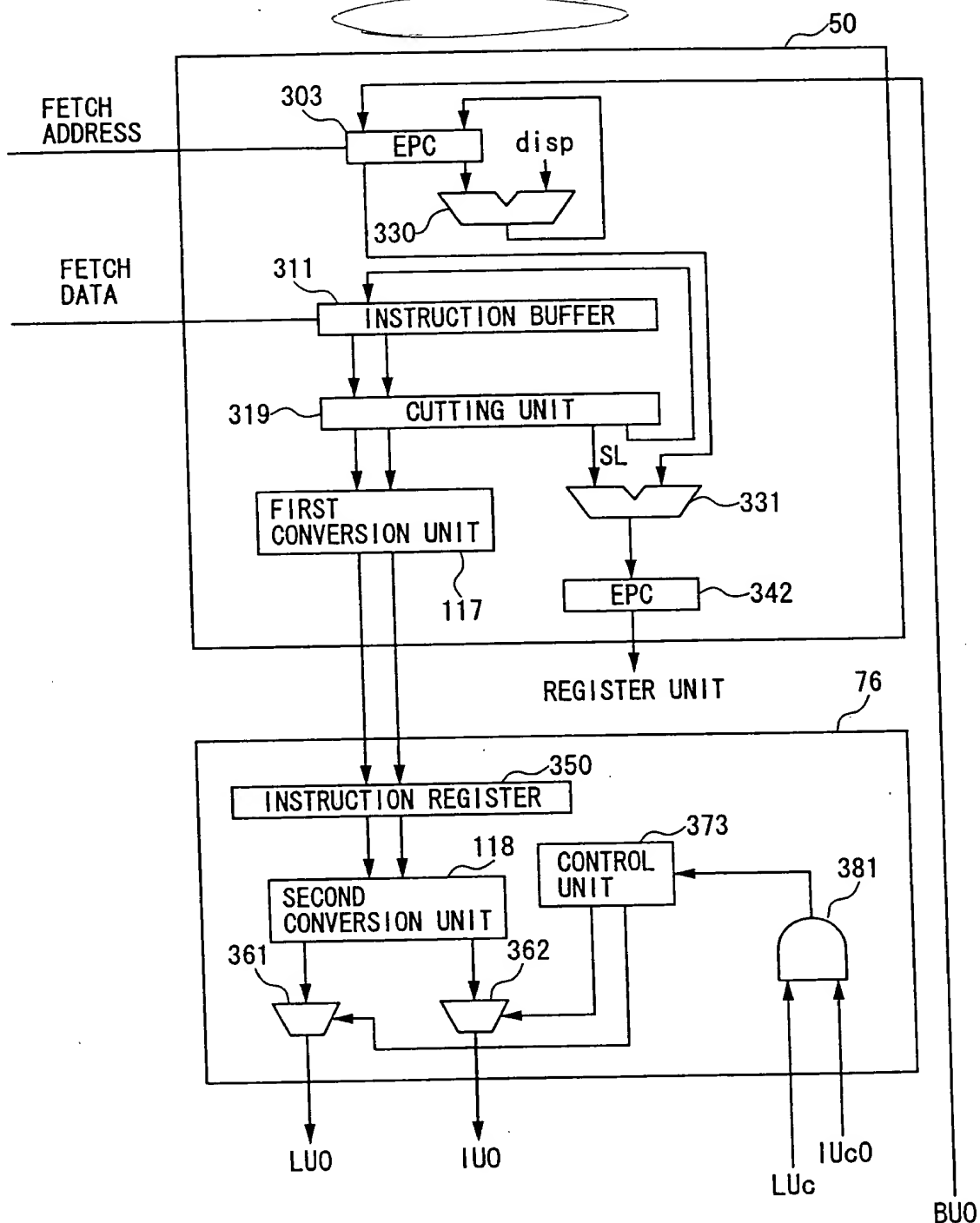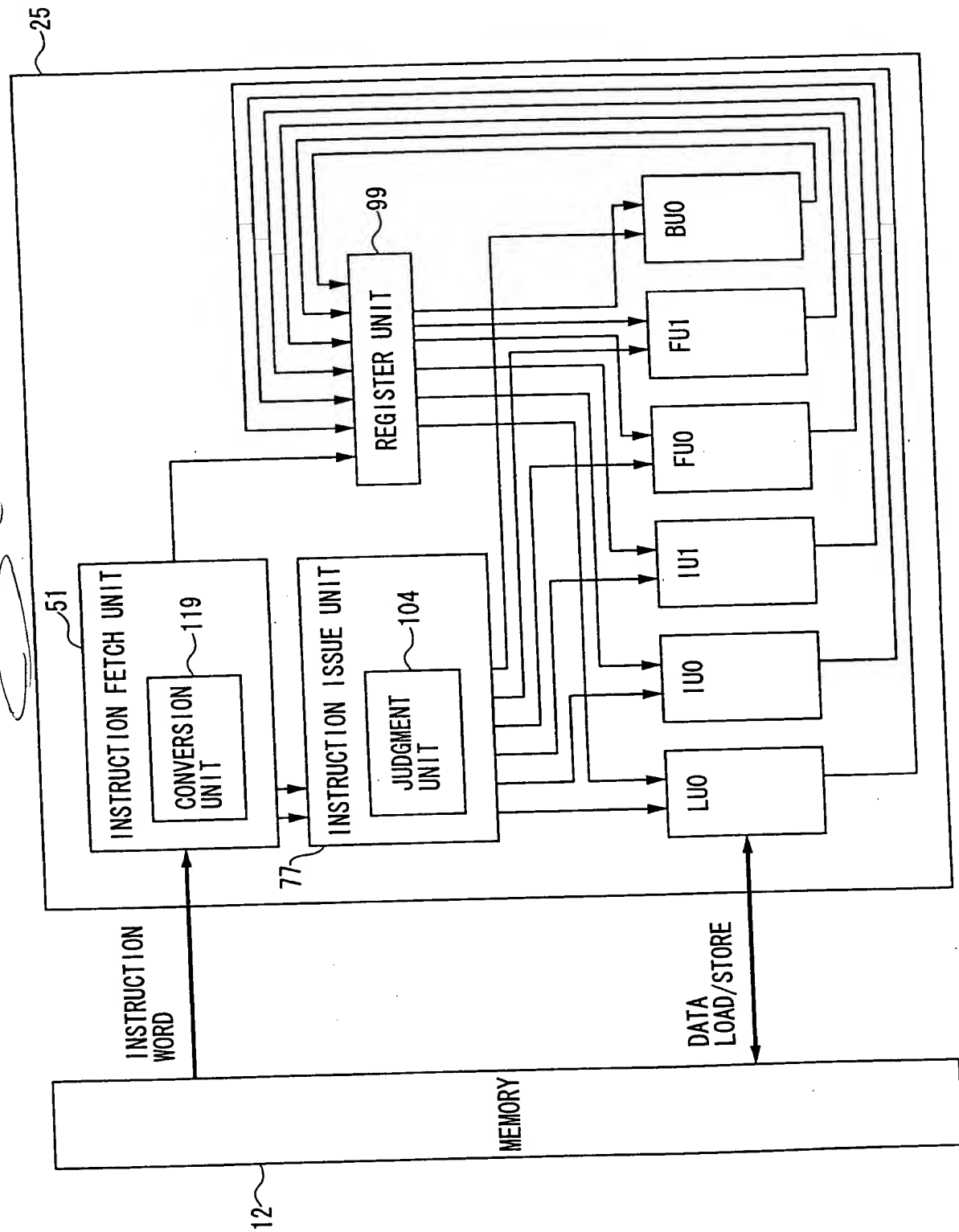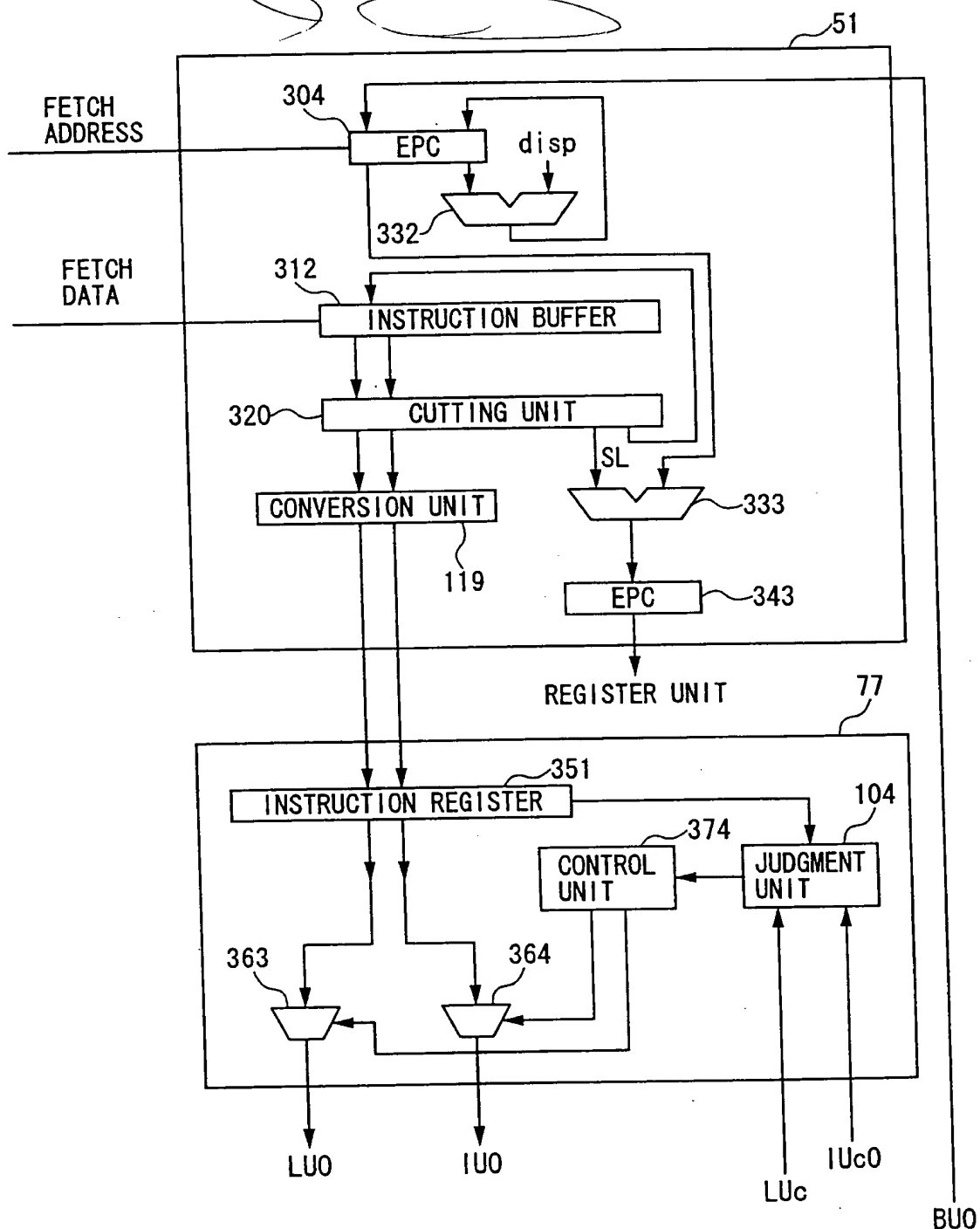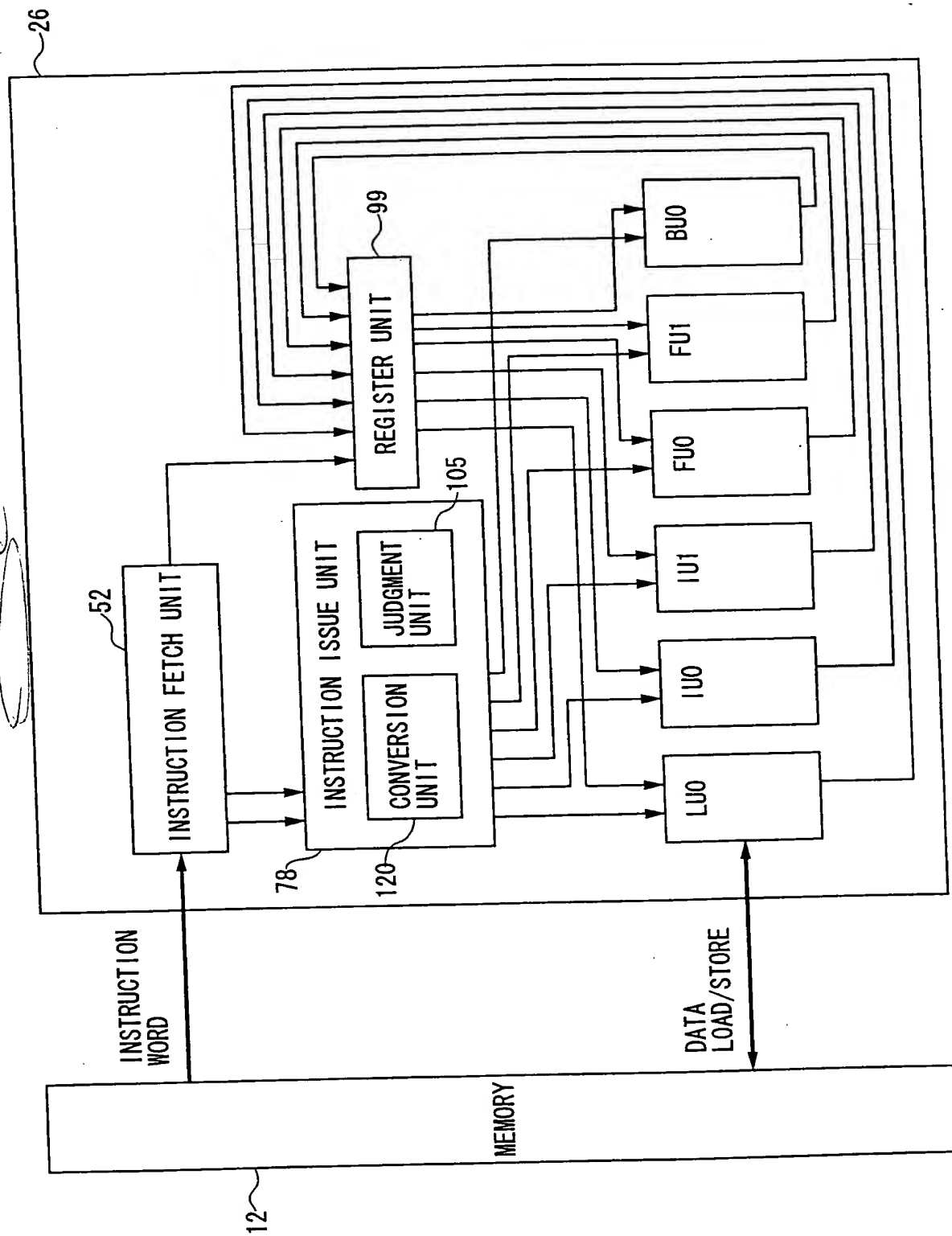in accordance with the second embodiment of the present

invention

FIG.12

FIG.13

49

FETCH
ADDRESS

302

EPC disp

328

FETCH
DATA

310

INSTRUCTION BUFFER

318 CUTTING UNIT

SL

329

EPC 341

REGISTER UNIT 75

349

INSTRUCTION REGISTER

116 CONTROL
UNIT 372 380

CONVERSION UNIT

359 360

LU0 IU0 IUc0 BU0

LUc

[FIG. 13]

Structures of an instruction fetch unit and an
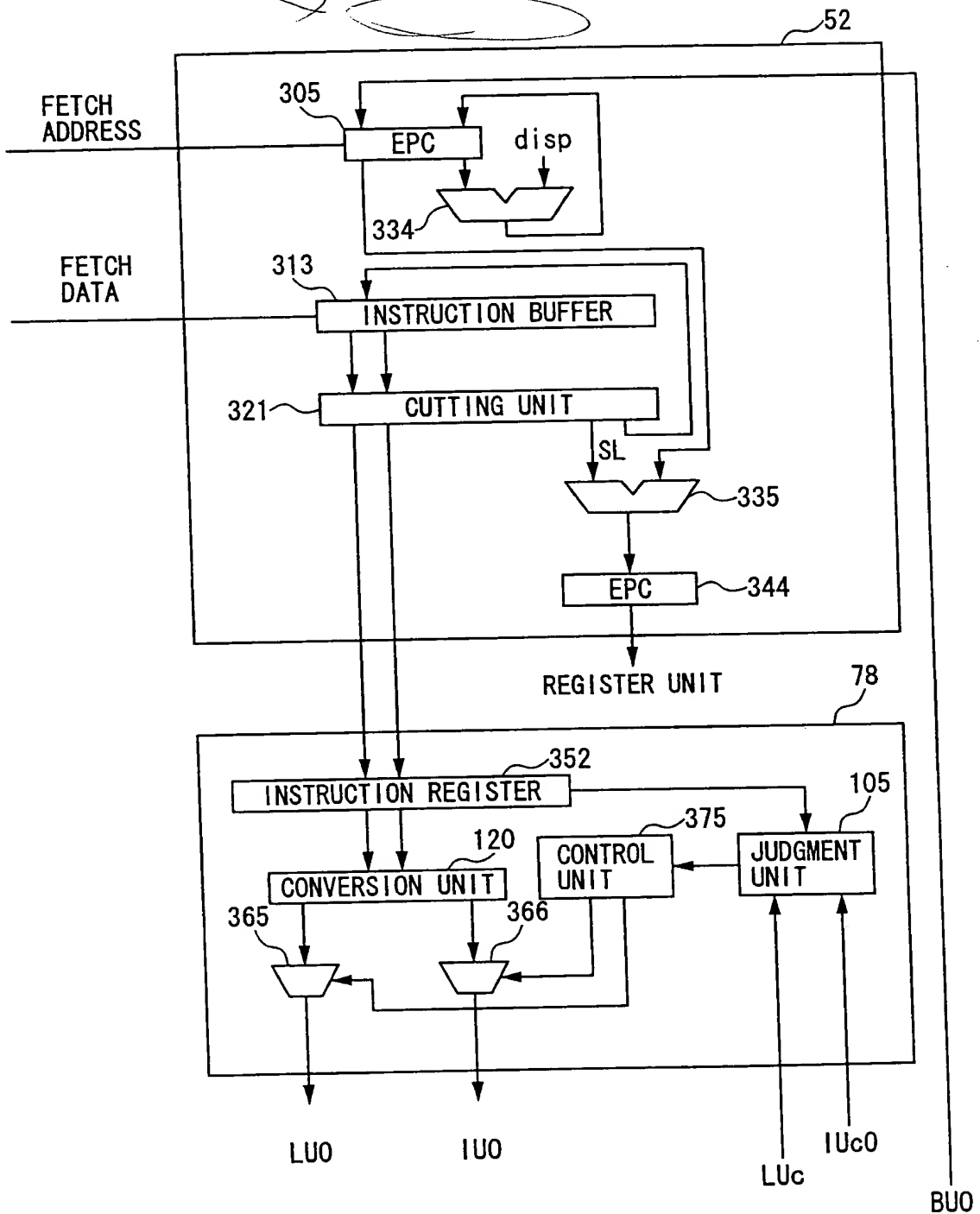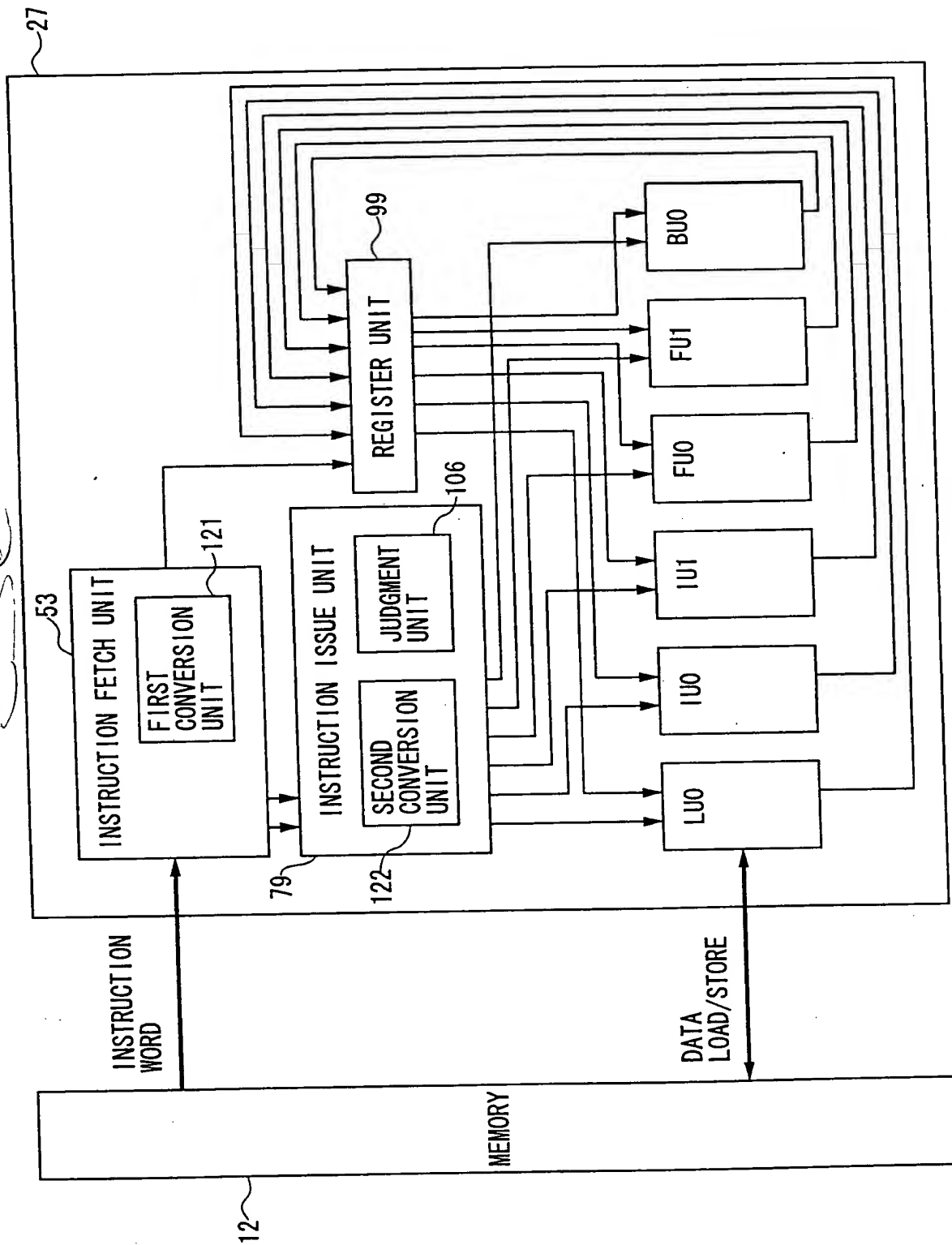instruction issue unit of the parallel processor shown
in FIG. 12

[FIG. 14]

Structure of a third example of the parallel processor

in accordance with the second embodiment of the present

invention

FIG.14

INSTRUCTION WORD

MEMORY

DATA LOAD/STORE

INSTRUCTION FETCH UNIT

FIRST CONVERSION UNIT — 117

INSTRUCTION ISSUE UNIT

SECOND CONVERSION UNIT — 118

REGISTER UNIT

BU0

FU1

FU0

IU1

IU0

LU0

24

50

76

99

12

[FIG. 15]

Structures of an instruction fetch unit and an
instruction issue unit of the parallel processor shown
in FIG. 14

FIG.15

[FIG. 16]

Structure of a fourth example of the parallel processor

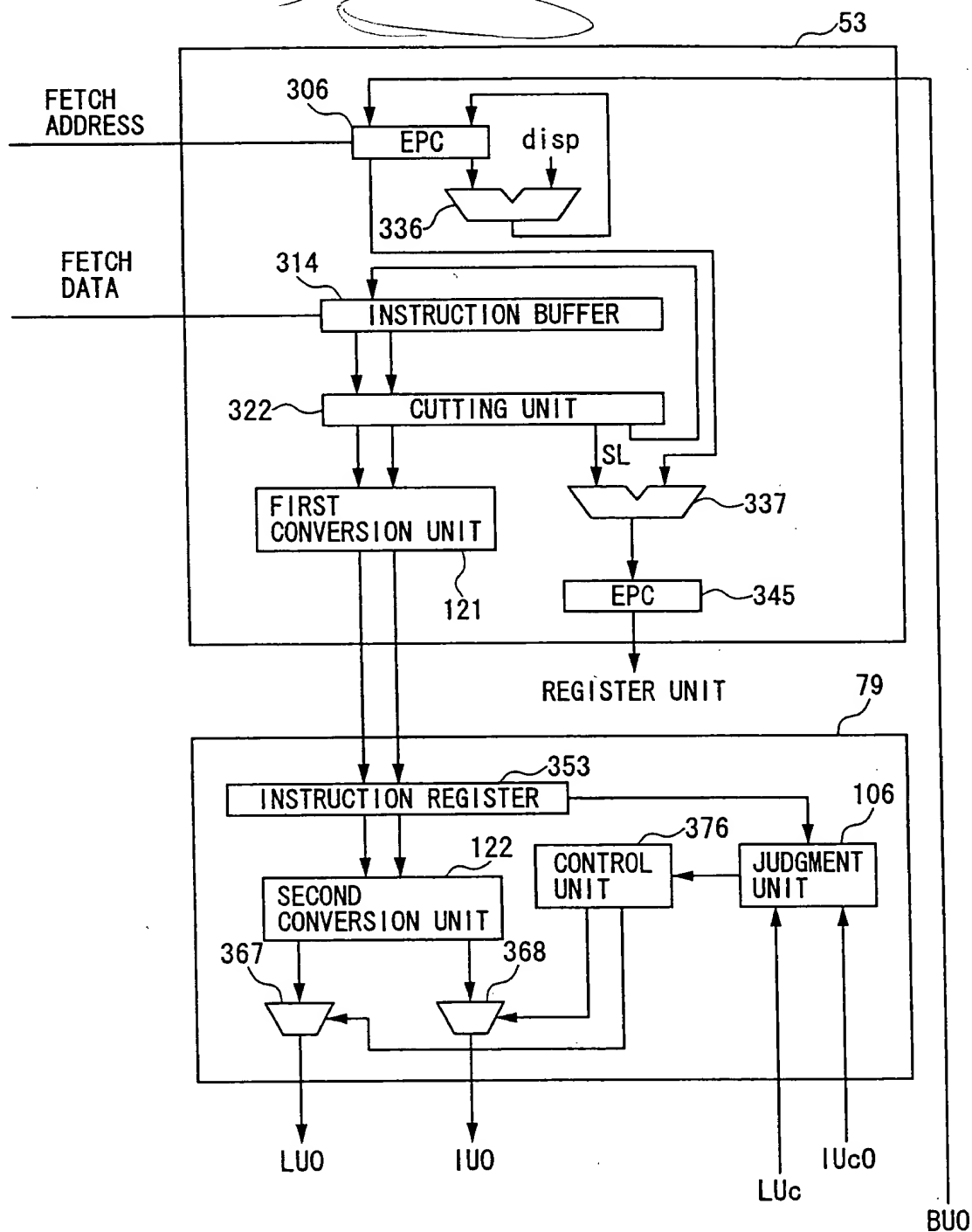in accordance with the second embodiment of the present

invention

FIG.16

[FIG. 17]

Structures of an instruction fetch unit and an
instruction issue unit of the parallel processor shown
in FIG. 16

FIG.17

[FIG. 18]

Structure of a fifth example of the parallel processor

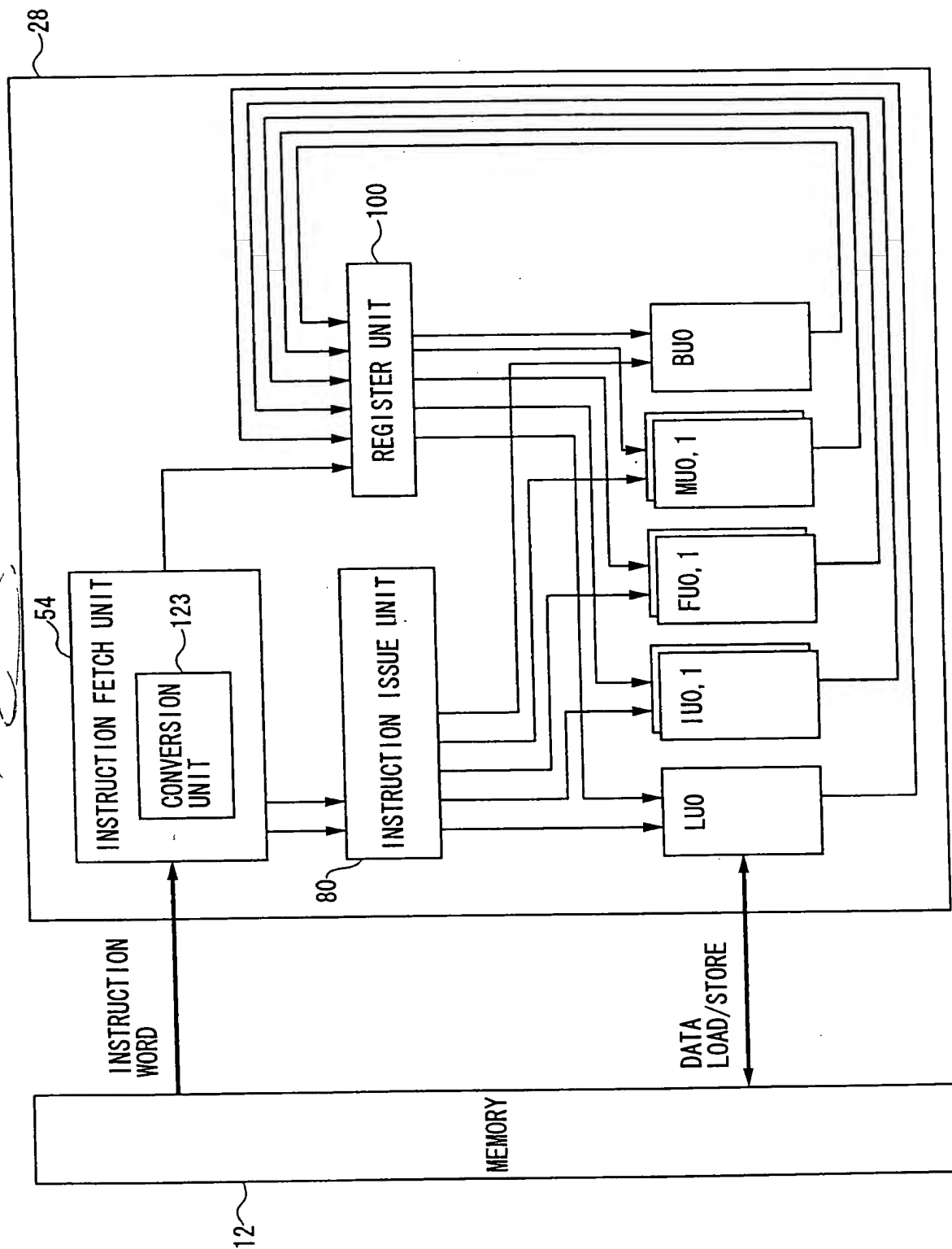in accordance with the second embodiment of the present

invention

FIG.18

26

52 INSTRUCTION FETCH UNIT

78 INSTRUCTION ISSUE UNIT

120 CONVERSION UNIT

105 JUDGMENT UNIT

99 REGISTER UNIT

LU0 IU0 IU1 FU0 FU1 BU0

INSTRUCTION WORD

DATA LOAD/STORE

MEMORY

12

[FIG. 19]

Structures of an instruction fetch unit and an
instruction issue unit of the parallel processor shown
in FIG. 18

FIG.19

FETCH
ADDRESS   305

EPC   disp

334

FETCH
DATA   313

INSTRUCTION BUFFER

321   CUTTING UNIT

SL   335

EPC   344

REGISTER UNIT   78

INSTRUCTION REGISTER   352

CONTROL   375   JUDGMENT   105
UNIT   UNIT

CONVERSION UNIT   120

365   366

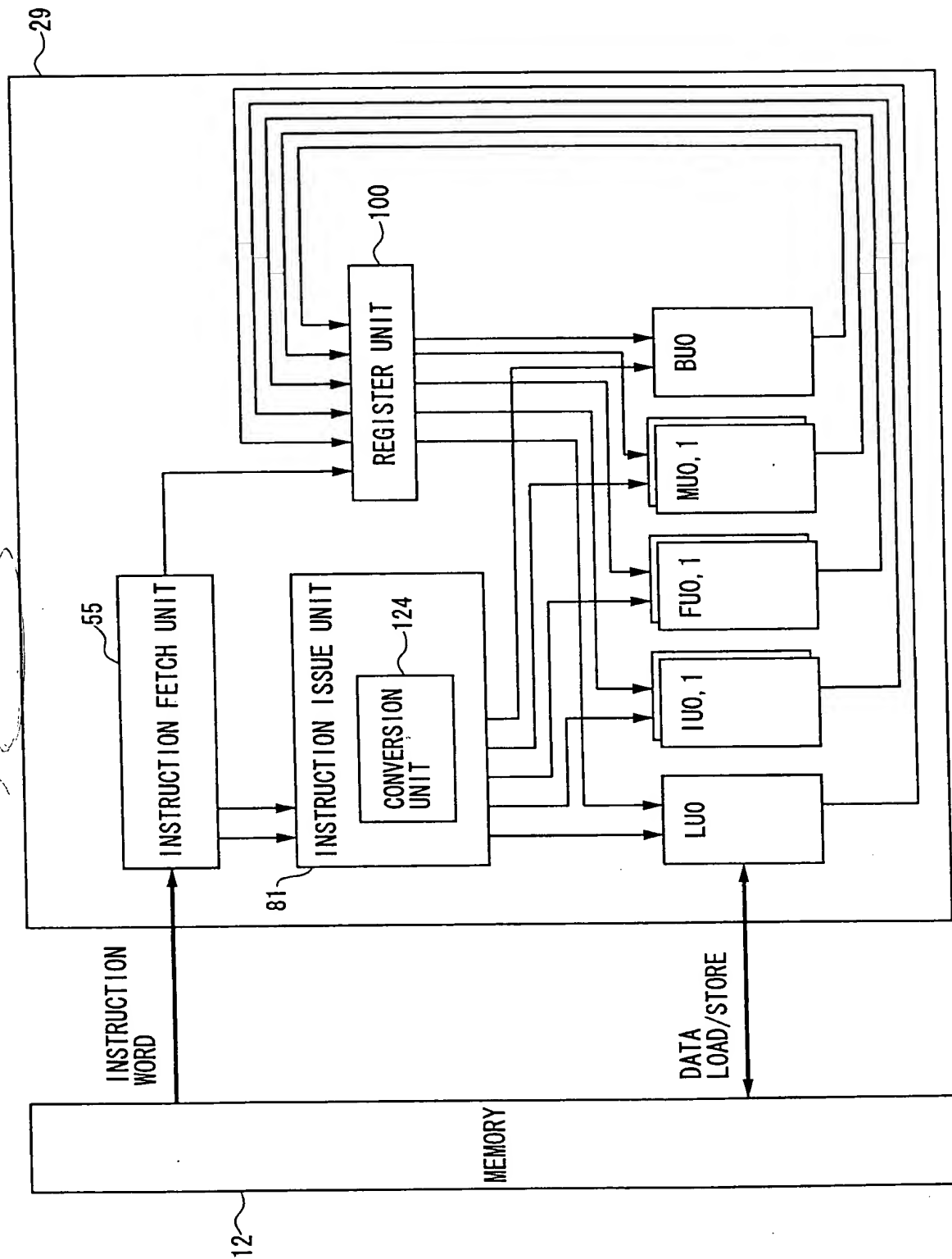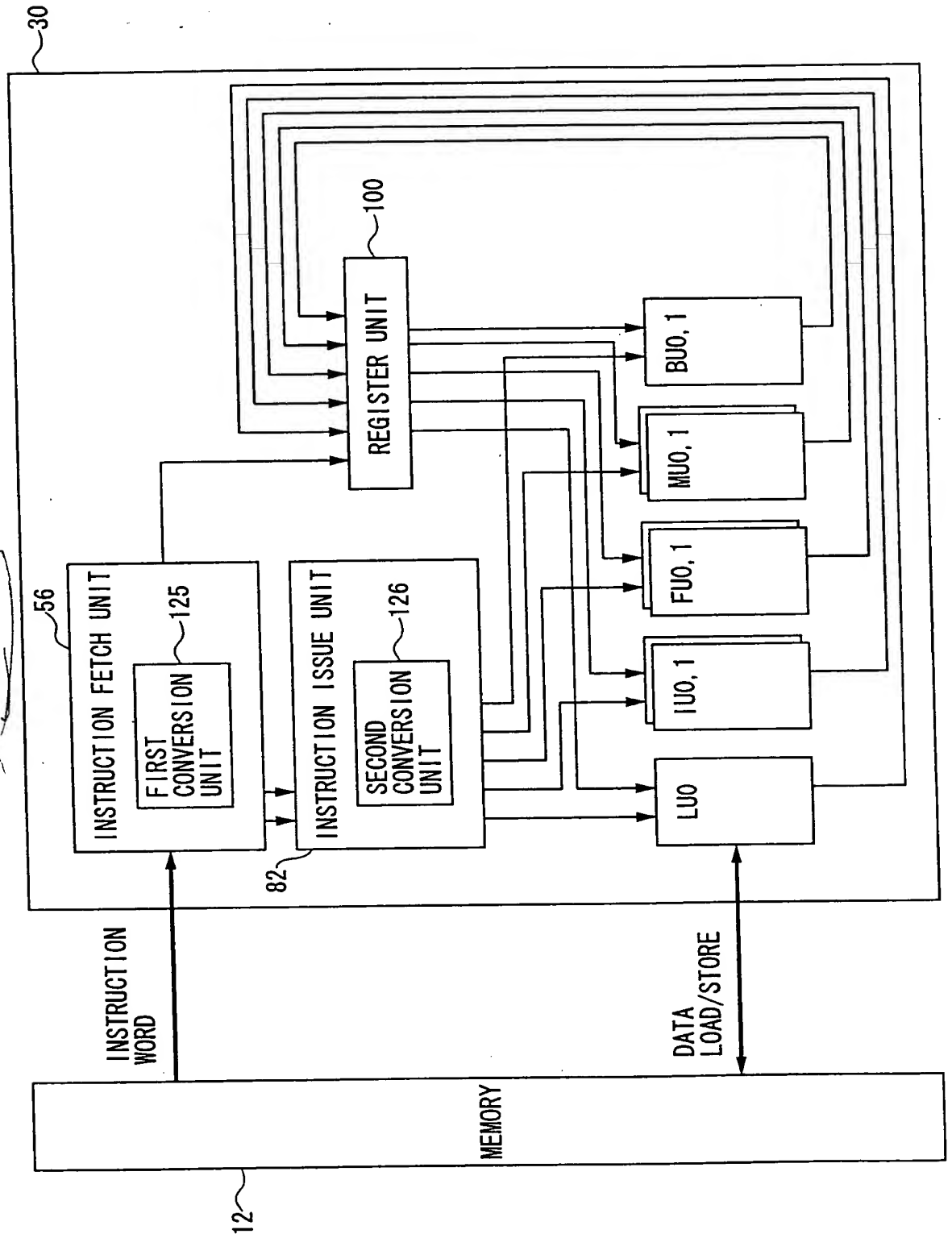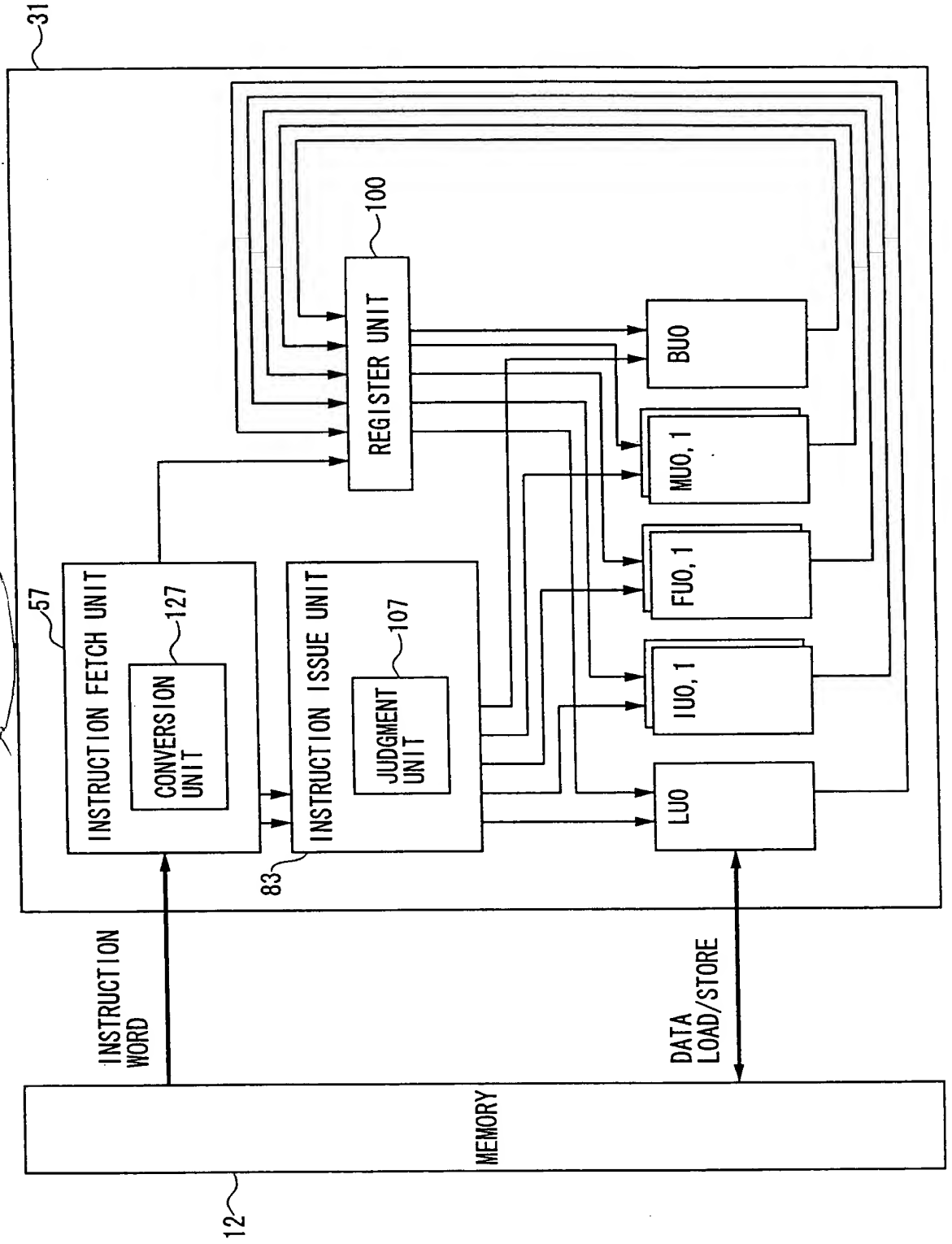LU0   IU0   IUc0

LUc   BU0

[FIG. 20]

Structure of a sixth example of the parallel processor

in accordance with the second embodiment of the present

invention

FIG.20

INSTRUCTION WORD

MEMORY

DATA LOAD/STORE

INSTRUCTION FETCH UNIT

FIRST CONVERSION UNIT

INSTRUCTION ISSUE UNIT

SECOND CONVERSION UNIT

JUDGMENT UNIT

REGISTER UNIT

LU0

IU0

IU1

FU0

FU1

BU0

27

53

121

79

122

106

99

12

[FIG. 21]

Structures of an instruction fetch unit and an

instruction issue unit of the parallel processor shown

in FIG. 20

FIG.21

[FIG. 22]

Structure of a first example of a parallel processor in accordance with a third embodiment of the present invention;

FIG.22

[FIG. 23]

Structure of a second example of the parallel processor

in accordance with the third embodiment of the present

invention

FIG.23

[FIG. 24]

Structure of a third example of the parallel processor

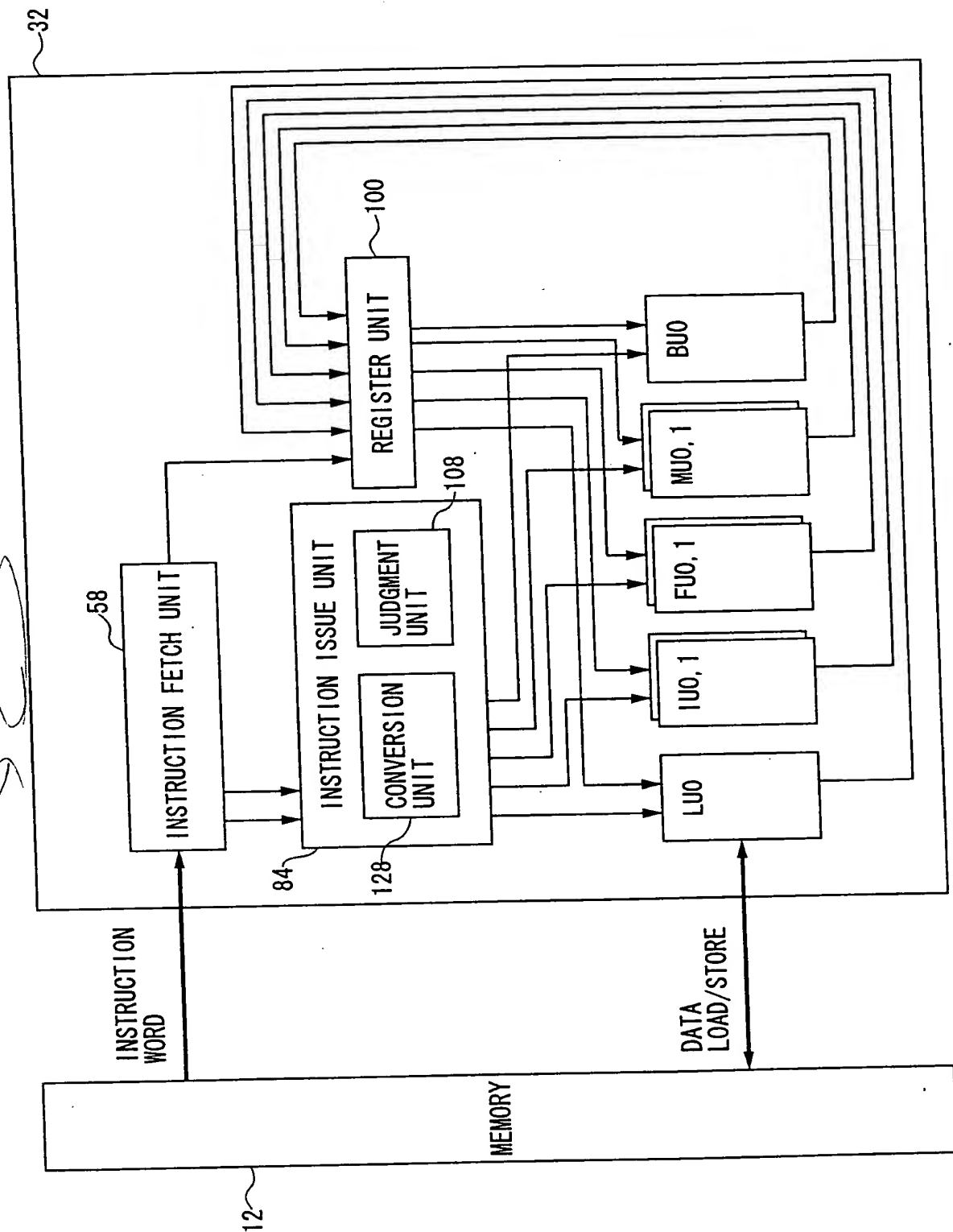in accordance with the third embodiment of the present

invention

FIG.24

INSTRUCTION WORD

MEMORY

DATA LOAD/STORE

INSTRUCTION FETCH UNIT

FIRST CONVERSION UNIT ~125

INSTRUCTION ISSUE UNIT

SECOND CONVERSION UNIT ~126

REGISTER UNIT ~100
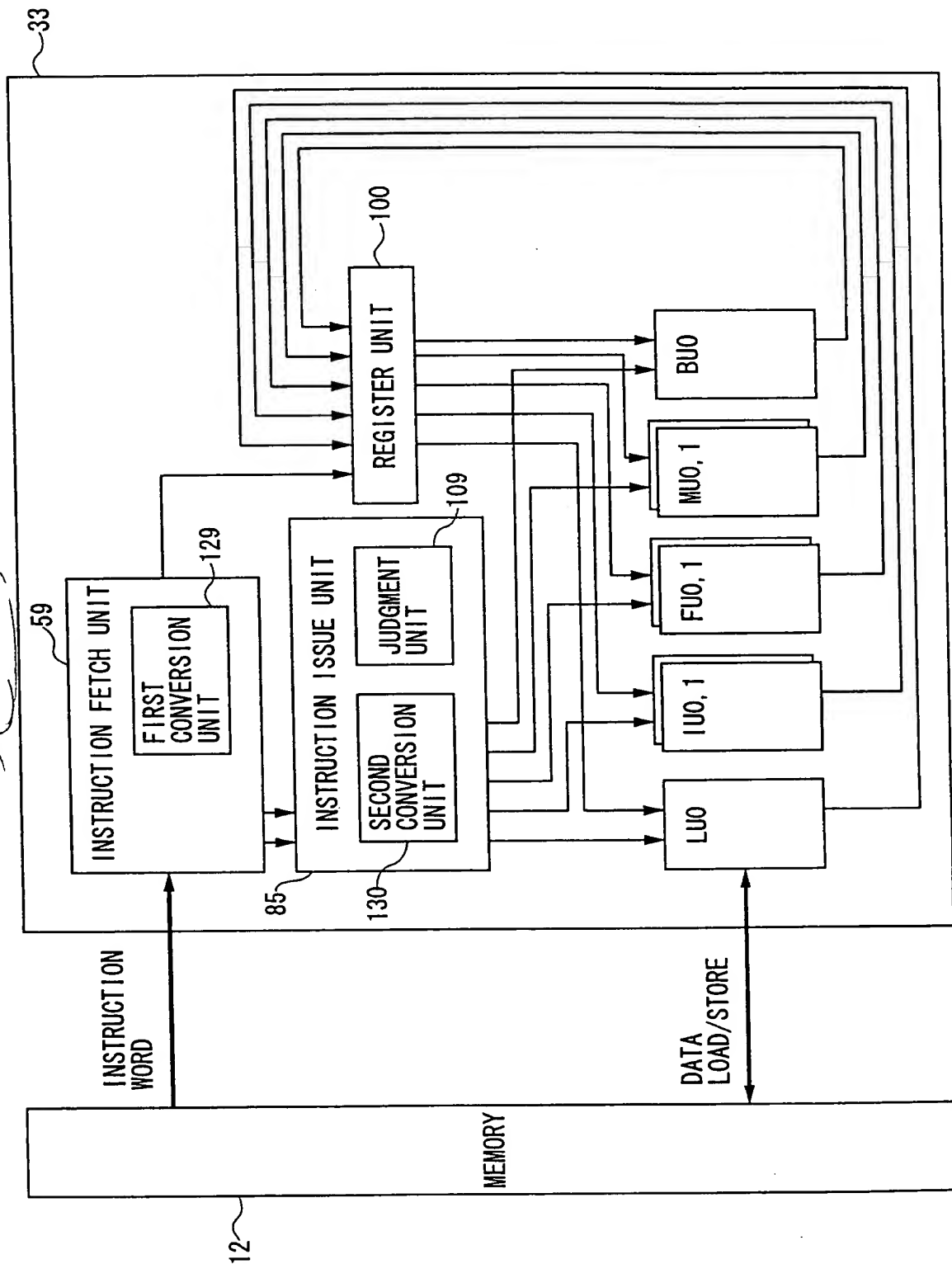
BU0,1

MU0,1

FU0,1

IU0,1

LU0

30

56

82

12

[FIG. 25]

Structure of a fourth example of the parallel processor

in accordance with the third embodiment of the present

invention

FIG.25

INSTRUCTION WORD

MEMORY

DATA LOAD/STORE

INSTRUCTION FETCH UNIT

CONVERSION UNIT

INSTRUCTION ISSUE UNIT

JUDGMENT UNIT

REGISTER UNIT
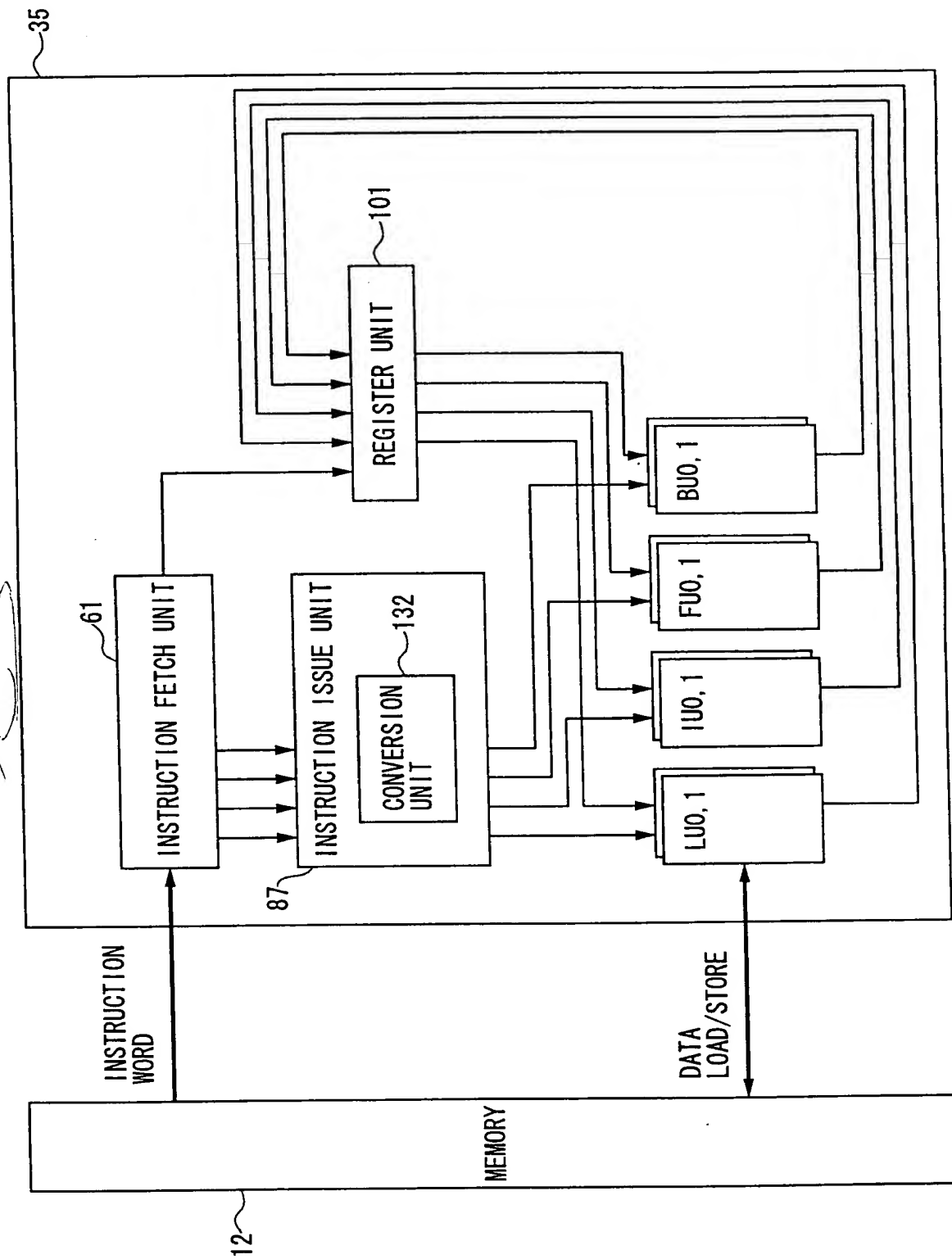
BU0

MU0, 1

FU0, 1

IU0, 1

LU0

31

57

127

83

107

100

12

[FIG. 26]

Structure of a fifth example of the parallel processor

in accordance with the third embodiment of the present

invention

FIG.26

MEMORY

INSTRUCTION WORD

DATA LOAD/STORE

INSTRUCTION FETCH UNIT

INSTRUCTION ISSUE UNIT

CONVERSION UNIT

JUDGMENT UNIT

REGISTER UNIT

LU0

IU0,1

FU0,1

MU0,1

BU0

[FIG. 27]

Structure of a sixth example of the parallel processor

in accordance with the third embodiment of the present

invention

FIG.27

33

INSTRUCTION WORD

INSTRUCTION FETCH UNIT   59

FIRST CONVERSION UNIT   129

INSTRUCTION ISSUE UNIT   85

SECOND CONVERSION UNIT   130

JUDGMENT UNIT   109

REGISTER UNIT   100

BU0

MU0, 1

FU0, 1

IU0, 1

LU0

DATA LOAD/STORE

MEMORY   12

[FIG. 28]

Structure of a first example of a parallel processor in
accordance with a fourth embodiment of the present
invention

FIG.28
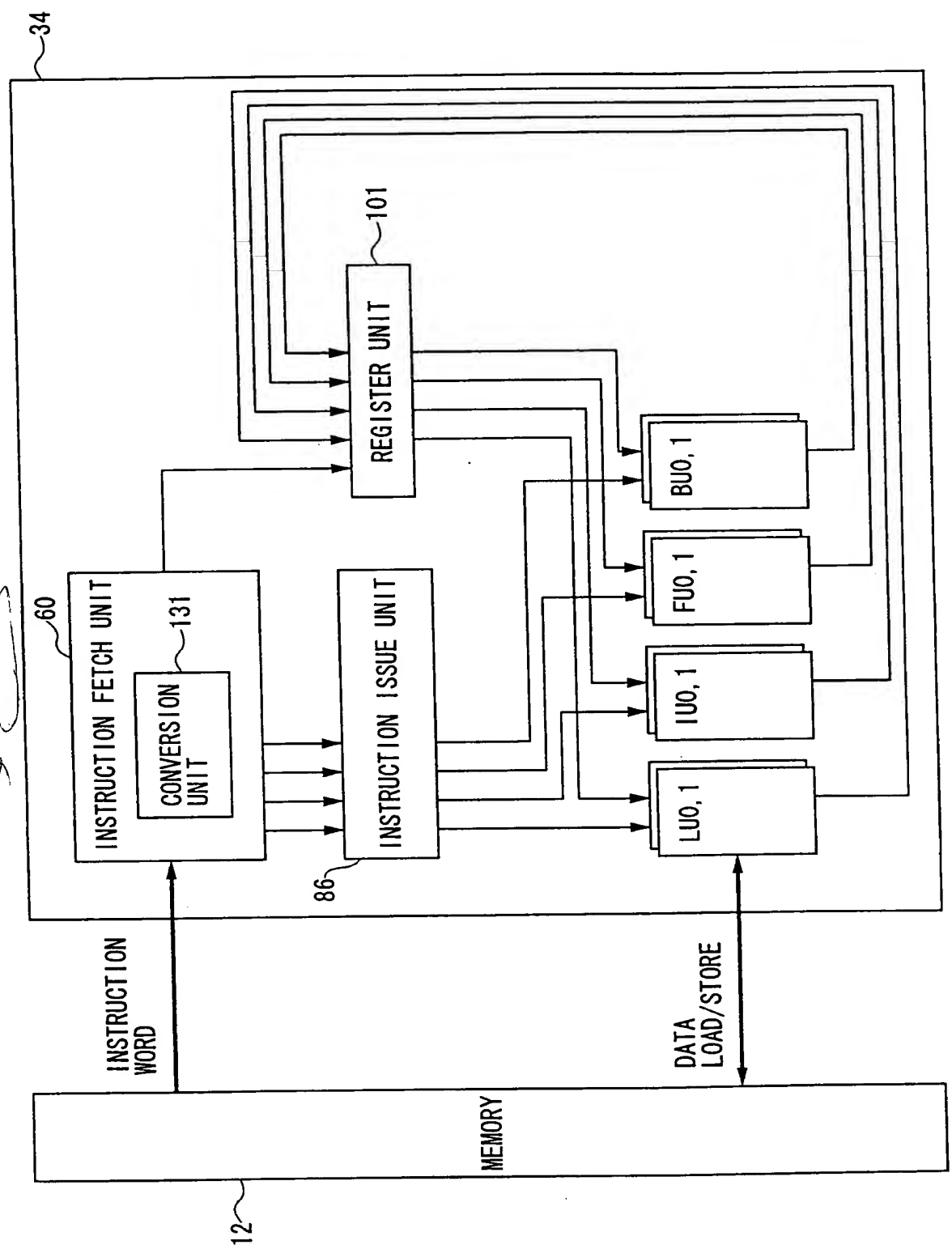
[FIG. 29]

Structure of a second example of the parallel processor

in accordance with the fourth embodiment of the present

invention

FIG.29

[FIG. 30]

Structure of a third example of the parallel processor

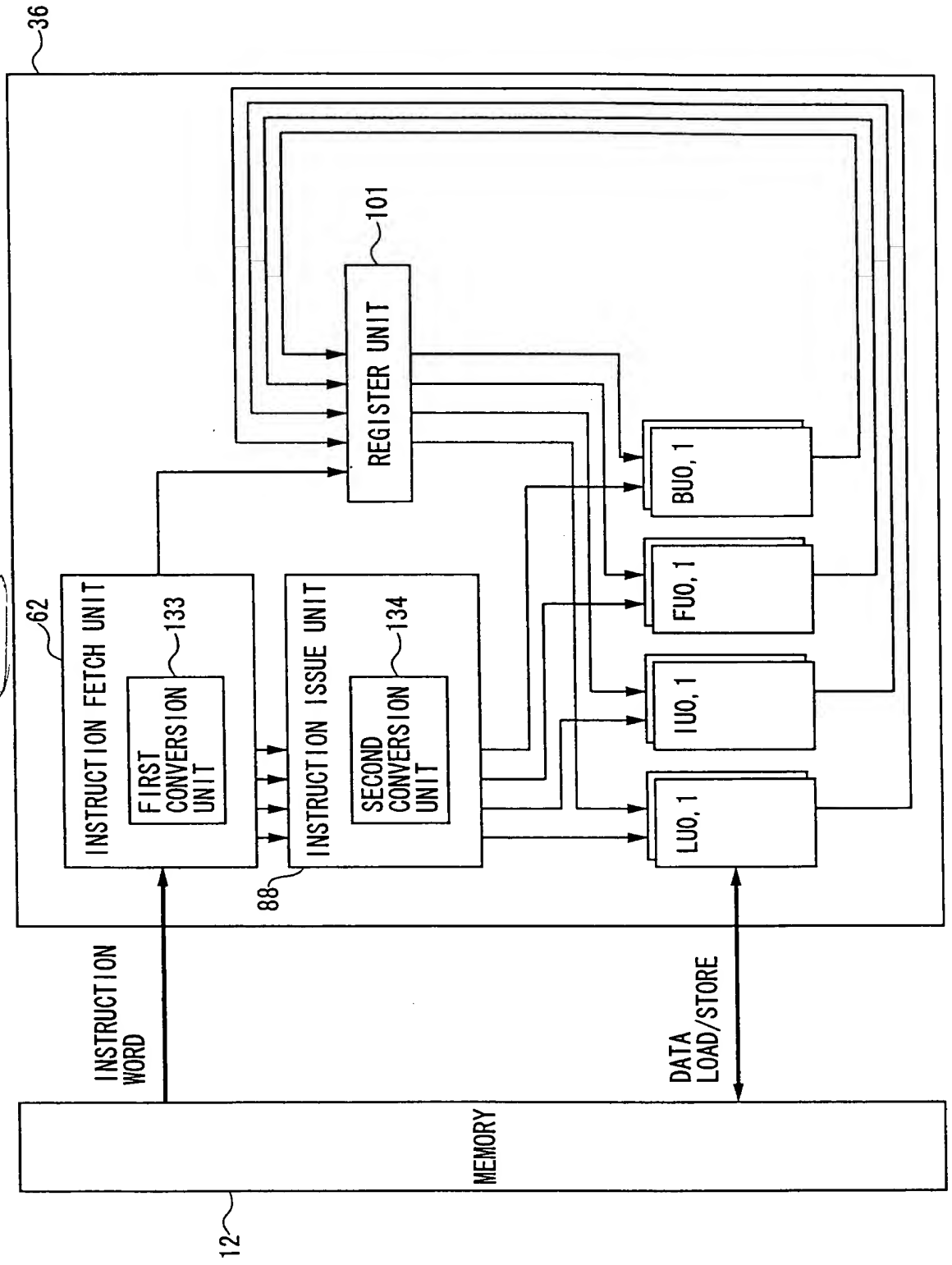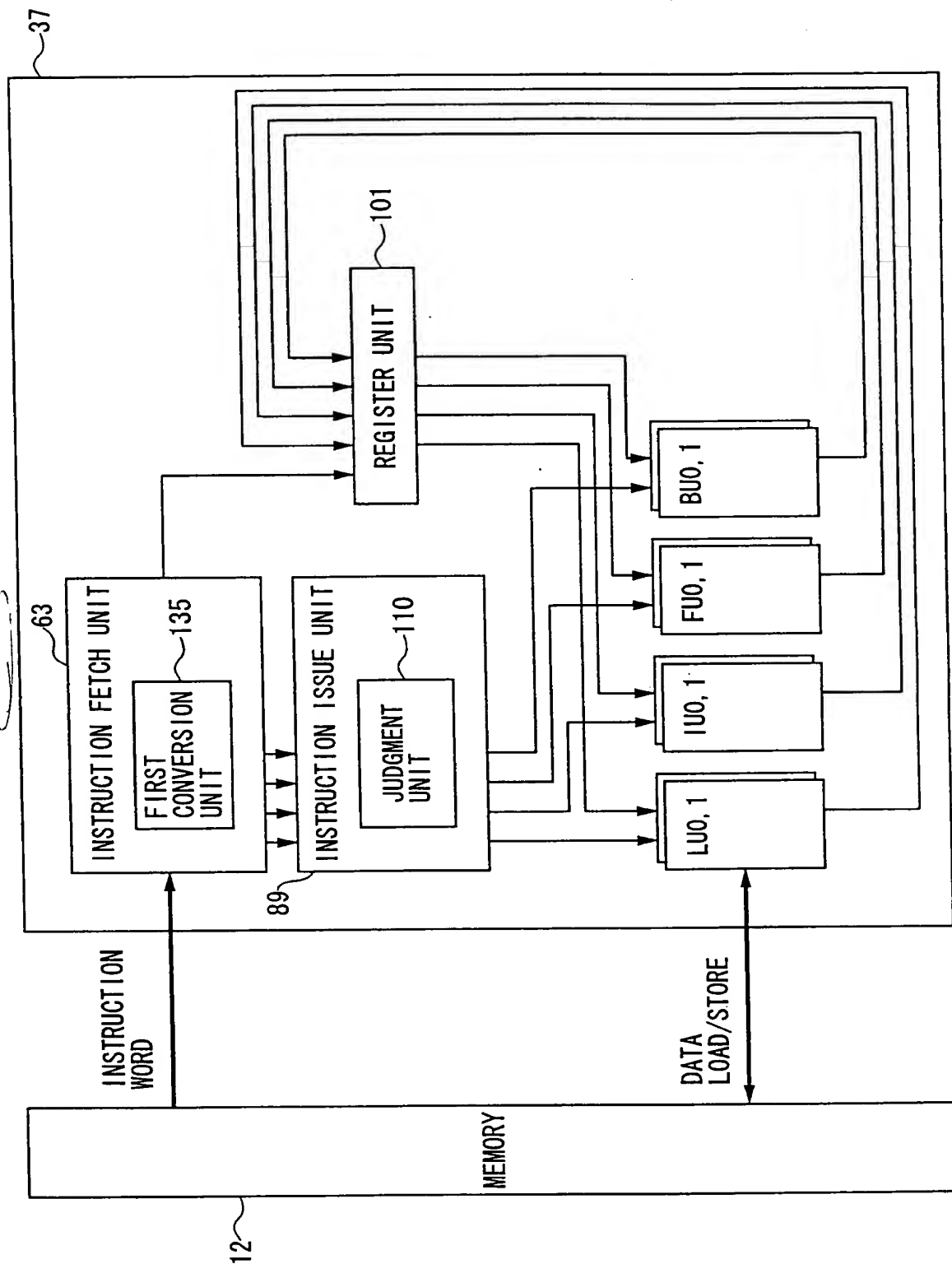in accordance with the fourth embodiment of the present

invention

FIG.30

MEMORY

INSTRUCTION WORD

DATA LOAD/STORE

INSTRUCTION FETCH UNIT

FIRST CONVERSION UNIT 133

INSTRUCTION ISSUE UNIT

SECOND CONVERSION UNIT 134

REGISTER UNIT 101

BU0, 1

FU0, 1

IU0, 1

LU0, 1

36

62

88

12

[FIG. 31]

Structure of a fourth example of the parallel processor
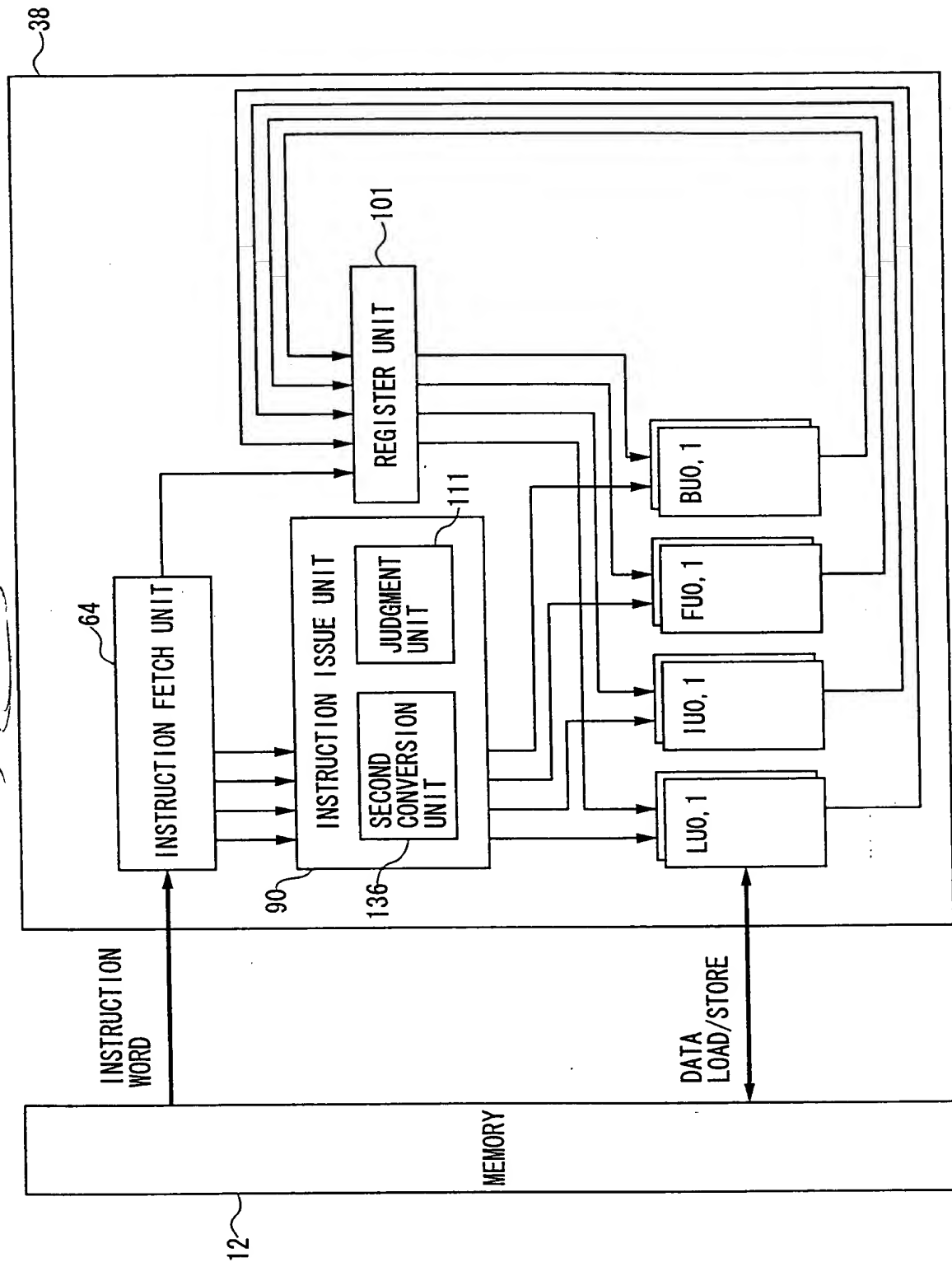in accordance with the fourth embodiment of the present
invention

FIG.31

[FIG. 32]

Structure of a fifth example of the parallel processor

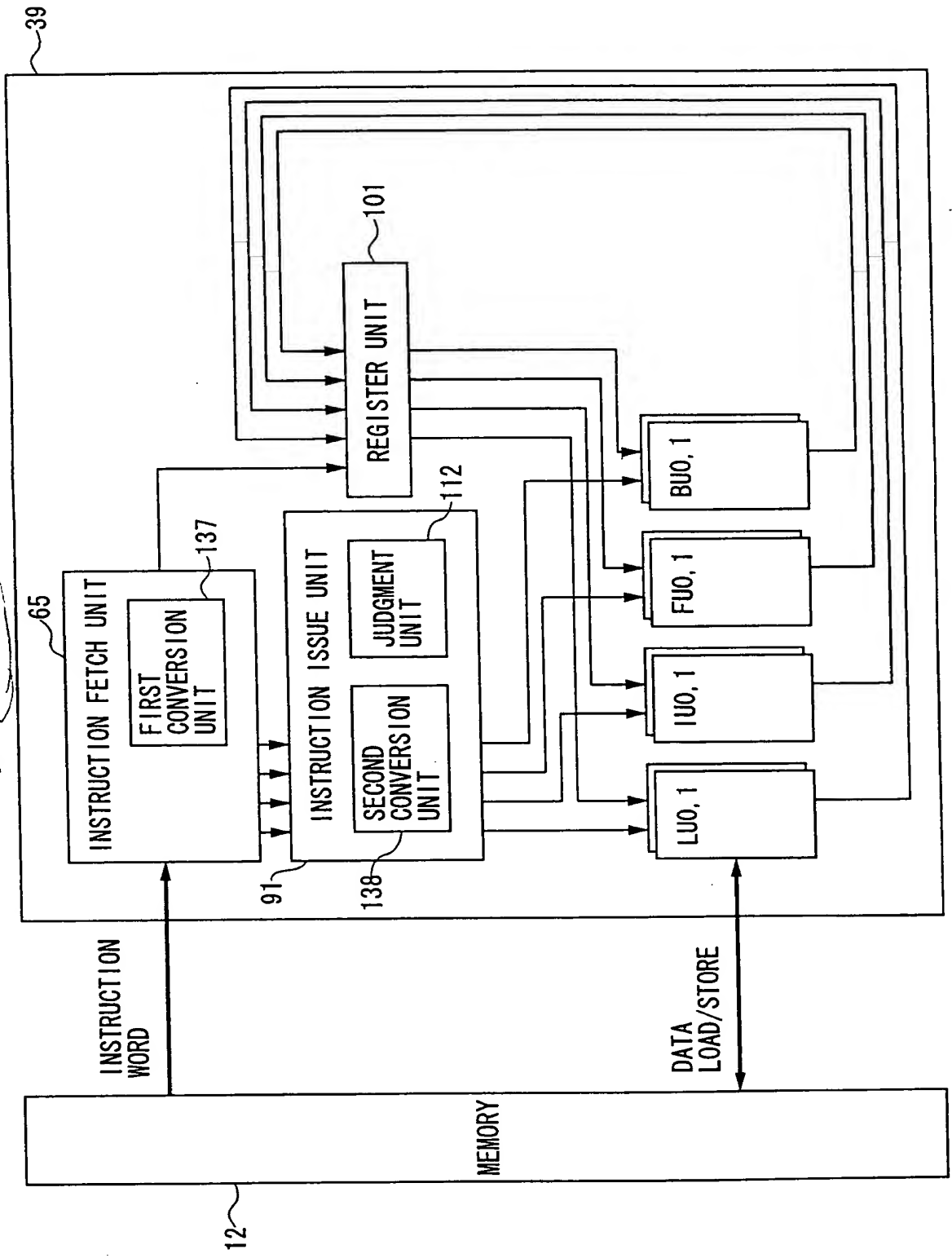in accordance with the fourth embodiment of the present

invention

FIG.32

INSTRUCTION WORD

INSTRUCTION FETCH UNIT 64

INSTRUCTION ISSUE UNIT 90

SECOND CONVERSION UNIT 136

JUDGMENT UNIT 111

REGISTER UNIT 101

BU0, 1

FU0, 1

IU0, 1

LU0, 1

DATA LOAD/STORE

MEMORY 12

38

[FIG.33]

Structure of a sixth example of the parallel processor

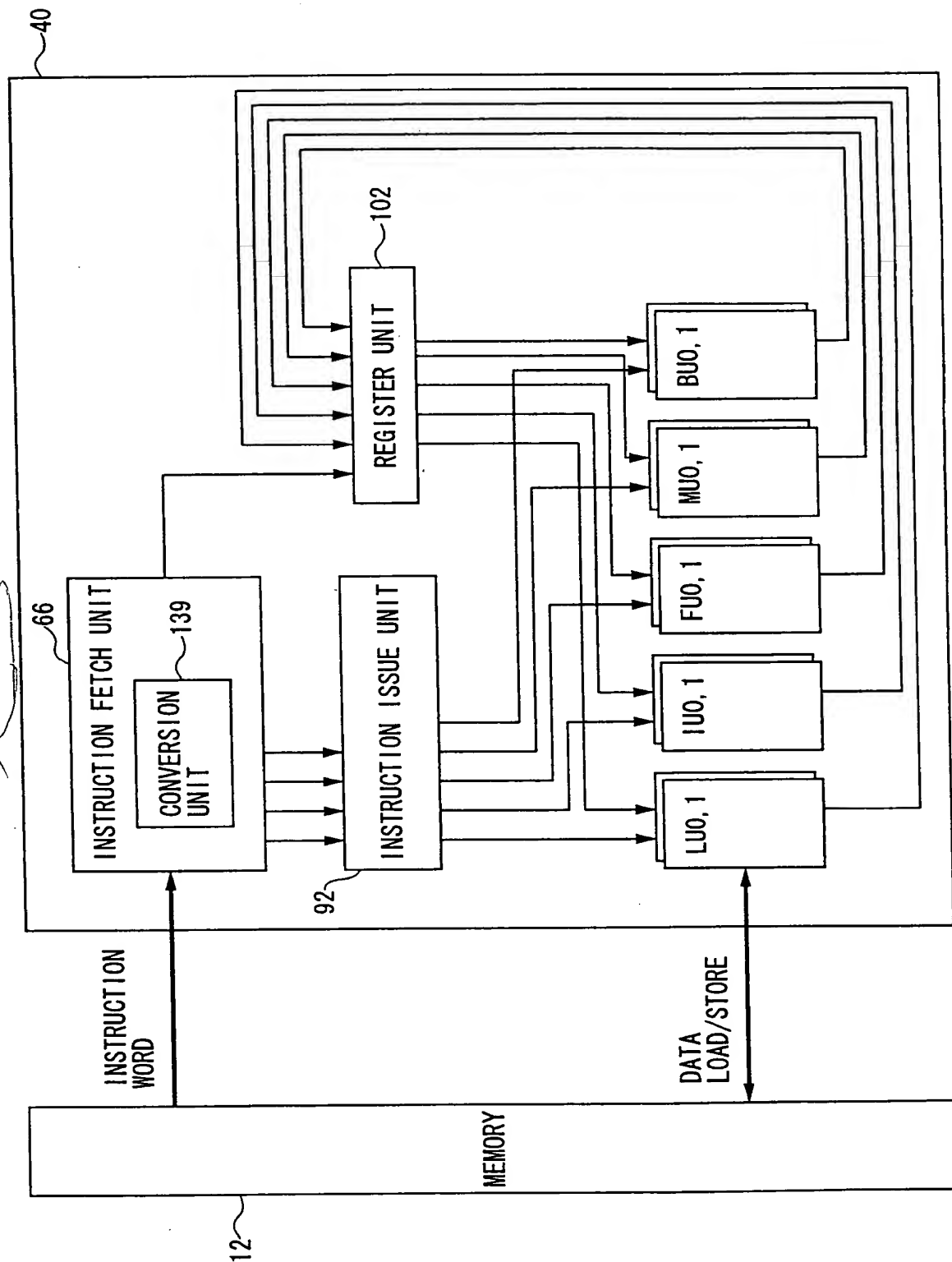in accordance with the fourth embodiment of the present

invention

FIG.33

[FIG. 34]

Structure of a first example of a parallel processor in accordance with a fifth embodiment of the present invention
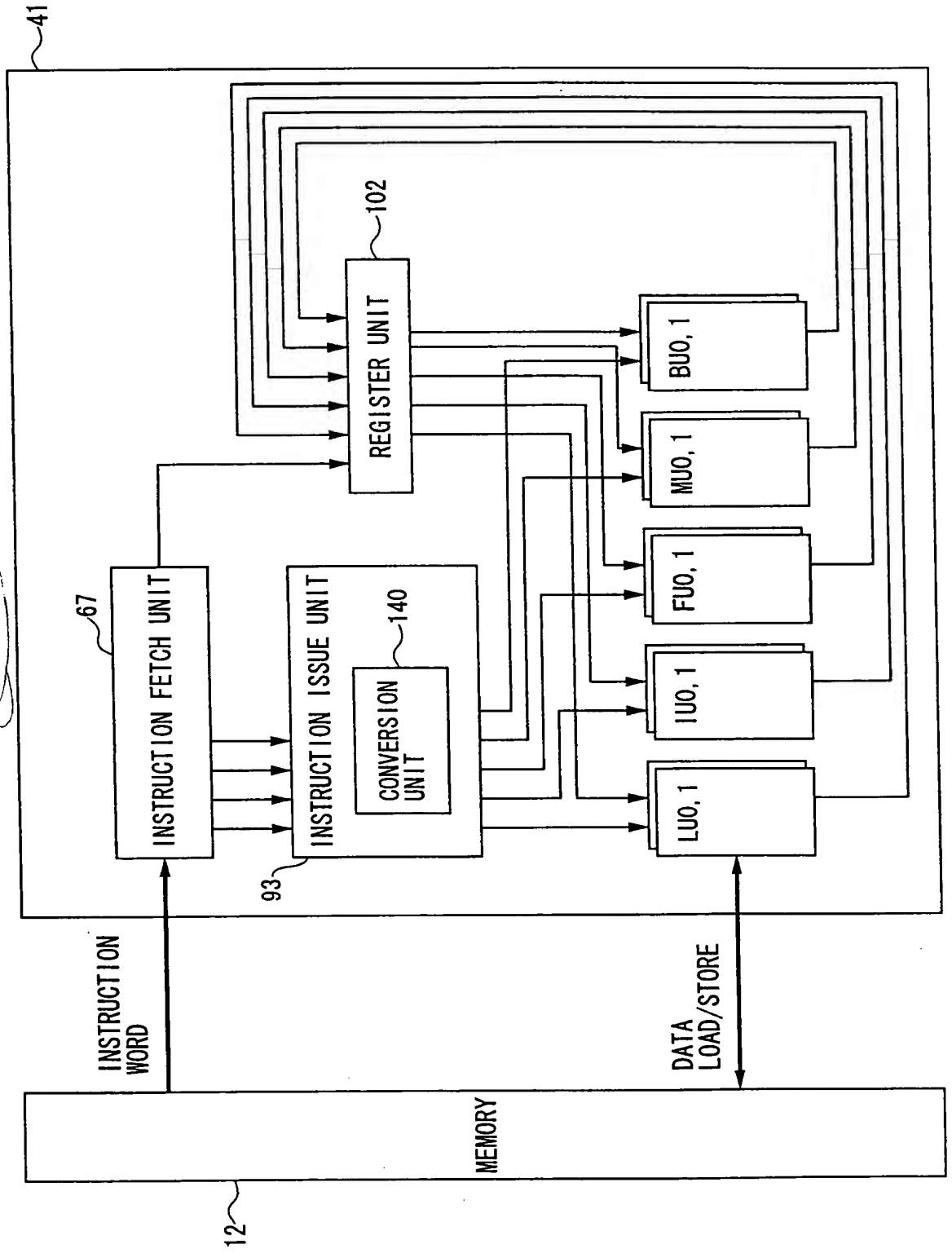
FIG.34

MEMORY — 12

INSTRUCTION WORD

DATA LOAD/STORE

INSTRUCTION FETCH UNIT — 66

CONVERSION UNIT — 139

INSTRUCTION ISSUE UNIT — 92

REGISTER UNIT — 102

40

BU0, 1
MU0, 1
FU0, 1
IU0, 1
LU0, 1

[FIG. 35]

Structure of a second example of the parallel processor

in accordance with the fifth embodiment of the present

invention

FIG.35

INSTRUCTION FETCH UNIT

INSTRUCTION ISSUE UNIT

CONVERSION UNIT

REGISTER UNIT

LU0, 1

IU0, 1

FU0, 1

MU0, 1

BU0, 1
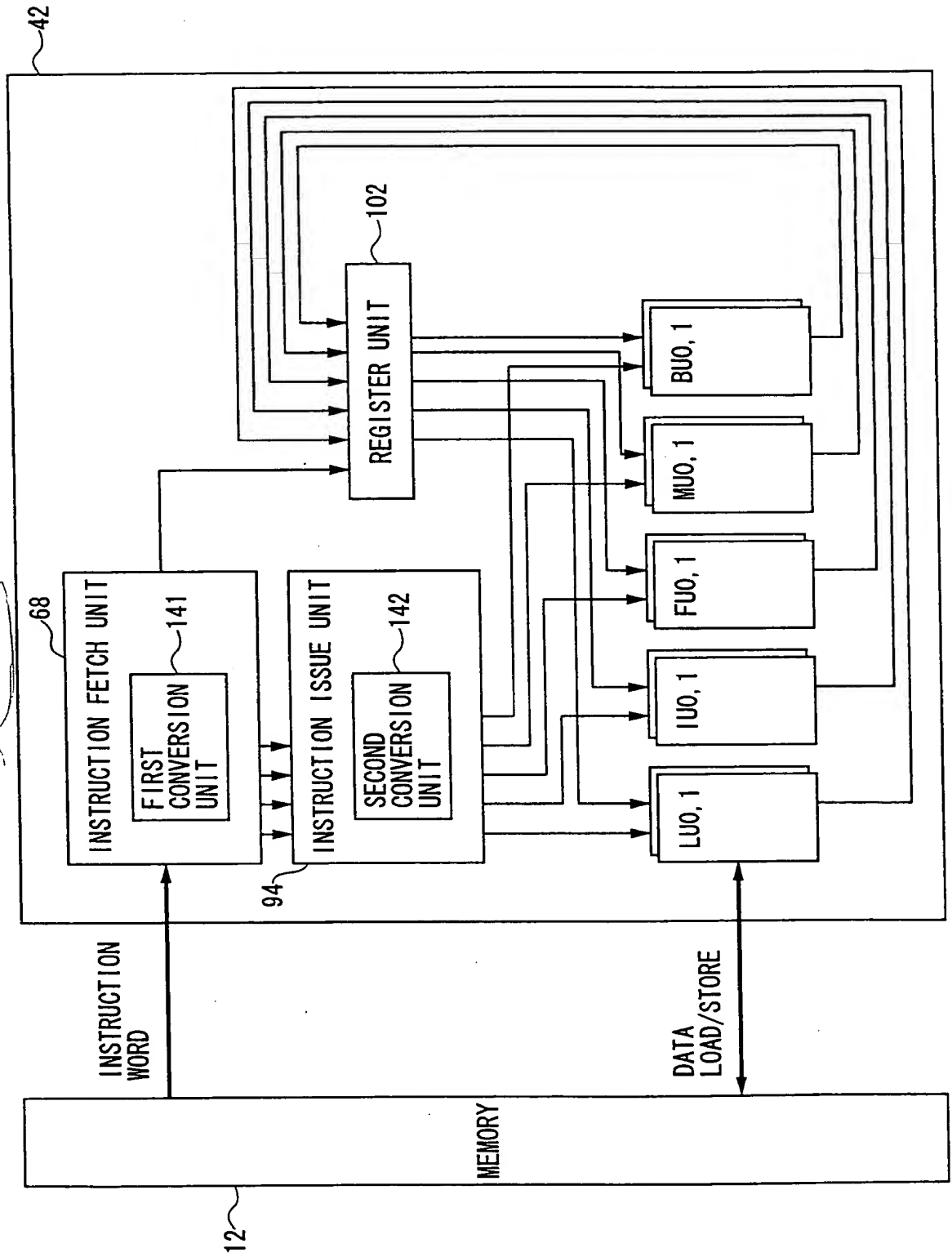
INSTRUCTION WORD

DATA LOAD/STORE

MEMORY

Structure of a third example of the parallel processor

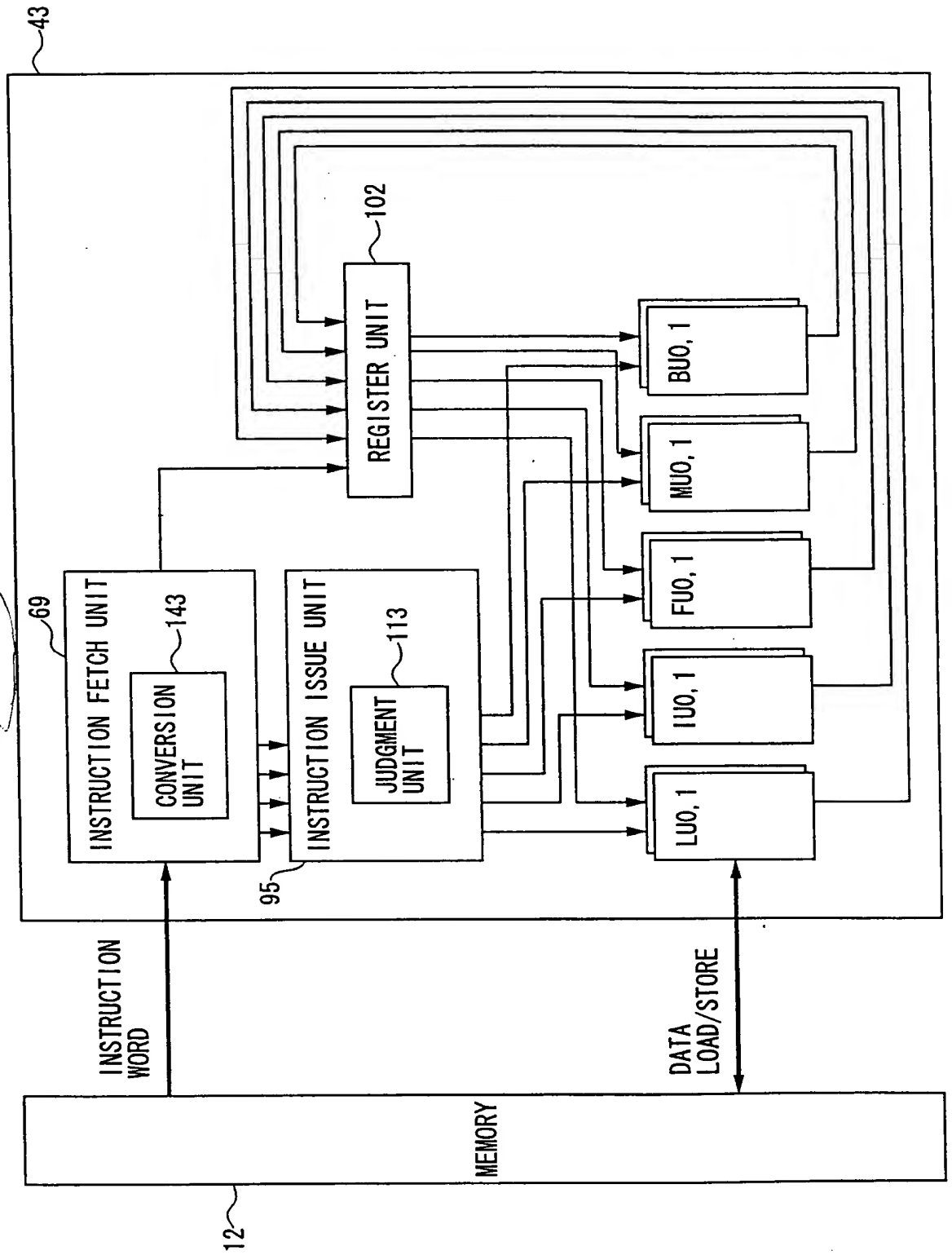in accordance with the fifth embodiment of the present

invention

FIG.36

[FIG.37]

Structure of a fourth example of the parallel processor

in accordance with the fifth embodiment of the present

invention

FIG.37

INSTRUCTION FETCH UNIT

CONVERSION UNIT — 143

69

INSTRUCTION ISSUE UNIT

JUDGMENT UNIT — 113

95

REGISTER UNIT — 102

43

LU0, 1

IU0, 1

FU0, 1
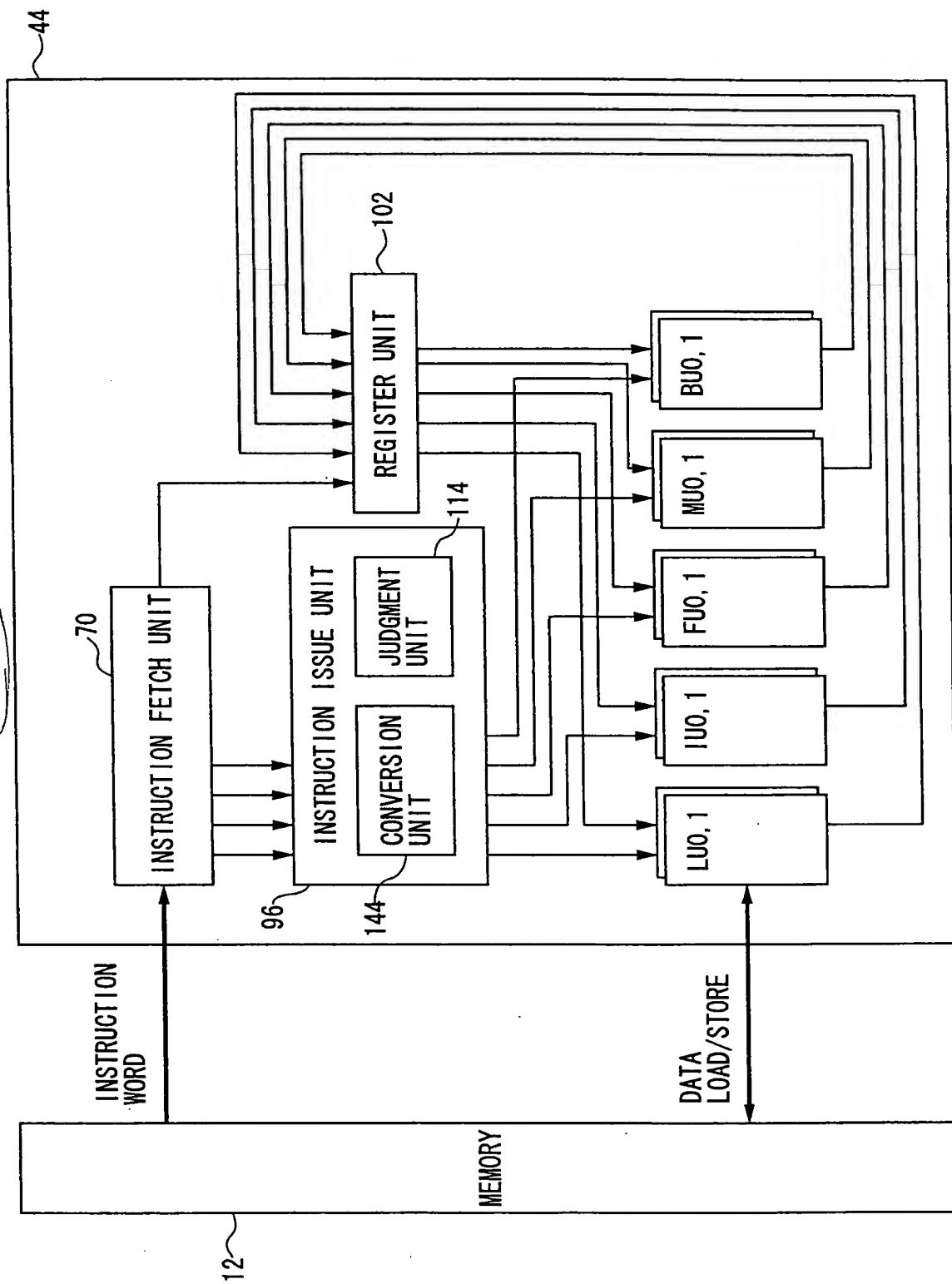
MU0, 1

BU0, 1

INSTRUCTION WORD

DATA LOAD/STORE

MEMORY

12

[FIG. 38]

Structure of a fifth example of the parallel processor

in accordance with the fifth embodiment of the present

invention

FIG.38

[FIG. 39]

Structure of a sixth example of the parallel processor

in accordance with the fifth embodiment of the present

invention

FIG.39

MEMORY

12

INSTRUCTION WORD

DATA LOAD/STORE

45

INSTRUCTION FETCH UNIT

71

FIRST CONVERSION UNIT

145

INSTRUCTION ISSUE UNIT

97

SECOND CONVERSION UNIT

146

JUDGMENT UNIT

219

REGISTER UNIT

102

LU0, 1

IU0, 1

FU0, 1

MU0, 1

BU0, 1